



PATENT
5298-04700/PM00028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

§ Group Art Unit: 1763

§ Examiner: Goudreau, G.

§ Atty. Dkt. No.: 5298-04700

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A
PLANARIZED SEMICONDUCTOR
STRUCTURE

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03
Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, William W.C. Koutny, Jr., hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

CONCEPTION

3. As supported below, I, along with Yitzhak Gilboa, Steven Hedayati and Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.
4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.
5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.
6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.
7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

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William W.C. Koutny, Jr.

Date: 7/10/03 _____

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO. PM 00028A. Name Yitzhak Glusker CY Initials Y/G Empl. No. 7395 Ext. No. 2719Citizenship US Dept # ICP Home Phone No. (408) 253-2577Home Mailing Address 1761 HERON AVE SCOTTSDALE AZ 85257B. Name William Buckley CY Initials B/B Empl. No. 135 Ext. No. 2673Citizenship 1 Dept # Home Phone No. (408) 253-2577Home Mailing Address 355 Homestead #45 San Jose, CA 95121
2225 Homestead #45 95121C. Name Steven Buckley CY Initials S/B Empl. No. 8534 Ext. No. 4556Citizenship US Dept # 3103 Home Phone No. (408) 927-0187Home Mailing Address 1240 Valley Quail Ct. San Jose CA 951202. TITLE OF INVENTION Method of making Shallow trench within Structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings

Redacted

Where can first drawing be found

Redacted

B. Date of first written description

Redacted

Where is description found

Redacted

C. Date of first oral disclosure to others

RedactedTo whom? Discussed with KTR, SSK, B/K

4. CONSTRUCTION OF DEVICE

A. Date Completed

B. Was prototype made?

C. By whom made?

D. Where can the prototype be found?

Inventor(s): Yitzhak Glusker Date 7/24/88Inventor(s): William Buckley Date 7/24/88Inventor(s): Steven Buckley Date 7/24/88Witnessed, Read, and Understood by: J. Sodick Date 8/24/88Witnessed, Read, and Understood by: J. Sodick Date 8/24/88

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO. _____

A. Name RanKumar CY Initials KTR Empl. No. 3305 Ext. No. 3720
Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031
Home Mailing Address 1193 LYNBROOK WAY ; SAN JOSE ; CA 95128

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

2. TITLE OF INVENTION

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings _____
Where can first drawing be found _____

B. Date of first written description _____
Where is description found _____

C. Date of first oral disclosure to others _____
To whom? _____

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B. Was prototype made? _____
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D. Where can the prototype be found? _____

Inventories: _____ Date: _____

Inventor(s): _____ Date: _____

Mentorship: _____ Date: _____

Witnessed, Read, and Understood by _____ Date _____

Witnessed Read and Understood by _____ Date _____

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Exhibit A- page 2

CYPRESS SEMICONDUCTOR

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5. TEST OF DEVICE

- A. Date: _____ Witness(es): _____
B. Results: _____

6. SALE

- A. Was invention sold or offered for sale? Yes No
B. Was invention used to make, assemble or test a commercial product? Yes No
C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes No
D. Actual or estimated date of first sale, offer or commercial use _____
E. Is invention part of a product for which there is a data sheet? Yes No (If yes, attach a copy)
F. Actual or estimated date of publication, release or availability of data sheet _____

7. USE

- A. Is invention presently being used? Yes No

- B. In what product or process is invention presently being used?

Are there specific plans for its use in near future? In what products or processes?

R&D

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS

5,972,792 / 4,010,573, and 5,782,675 / 5,919,022
4,393,627 / 5,782,675 / 5,919,022

9. WAS INVENTION Conceived (Yes No) Constructed (Yes No) Tested (Yes No) during performance of Government Contract?

Contract Number _____

(Give Full Contract Number)

=====

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s): Milton Weitz Date 8-3-91

Inventor(s): J. R. Jaiswal Date 8/12/91

Inventor(s): J. L. Lin Date 8/12/91

Witnessed Read, and Understood by: John G. Kish Date 8-3-91

Witnessed Read, and Understood by: U.S. Tech Date 8/12/91

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CYPRESS SEMICONDUCTOR

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FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available.
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

=====

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, by doing so reducing processing steps.
2. Current technology (87-102 TDS) calls for the following steps:

1. Invert 180° in PECVD, SiO₂, SiN_x, Si_xN_y, Film, Deposit
2. Etch SiO₂ using HCl to Leave SiN_x as mask

Inventor(s): William Mandy Date 3/24/02

Inventor(s): J. L. Sardis Date 3/24/02

Inventor(s): U. H. Jia Date 3/24/02

Witnessed, Read, and Understood by: John J. Mandy Date 3/24/02

Witnessed, Read, and Understood by: J. L. Sardis Date 3/24/02

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CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3) Disadvantages addressed by invention:

1. Thick nitride layer required to overcome TDDB limiting in poly cap.
2. Masking may include stress relief.
3. Extra steps after nitride strip which can result in Poly stringing.
4. thicker oxide film required to overcome any adhesion by nitride.

(4) The current invention has three options for using

Fixed fluorine poison as the ~~nitride~~ method of poison.

The main advantage of Fixed fluorine is the negligible amount of baking compared to conventional baking processes.

The second advantage is self-aligning after PECVD nitride remains after

Option I - No Nitride Hard mask

In this option we obtain that desired Film is poison on base and trench with no damage to PECVD step or even the trench is etched. After trench with oxide film is deposited in the trench and oxide film contains a thickness of the trench + trench depth variation of the oxide - Etchback the oxide is poisioned by fixed fluorine in a reduced thickness of 0-500 Å. The last two processes is a self-aligning after PECVD nitride remains after PECVD nitride remains after

Invention: nitride Hard Date: 8/26/01

Invention: I Gotoh Date: 8/28/01

Invention: J. H. Sodini Date: 2/29/01

Witnessed, Read and Understood by: J. H. Sodini Date: 2/28/01

Witnessed, Read and Understood by: J. H. Sodini Date: 2/28/01
Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Deposit Thin Nitride -

grow base oxide, grow thin layer of Nitride (0-500Å)
 expose Field Oxide mask, Etch nitride, Deposit SiN oxide
 polish down to ~~SiO₂~~ stop on oxide at a predetermined
 thickness oxide above the nitride. Stop remaining oxide.
 Stop remaining nitride.

Option III

grow base oxide deposit PEPSI/PSL, expose field
 Etch trench, deposit L. H. oxide, Polish to PEPSI/PSL height
 wet stop to remove remaining PEPSI, use Etch Rite
 wet stop to remove oxide, Due to use Etch Rite
 instances of deposit to new etched oxide due to
 result of previous step of nitride, may have to

- (6) To my knowledge of what I understand of the disclosure
 following the use of this it is suitable for this.
- (7) That the above is the true story about what I know concerning
 this product. I may be ignorant of things.

Inventor(s) John Murphy Date 5/24/02

Inventor(s) J. Hartog Date 5/24/02

Inventor(s) B. J. Clegg Date 5/24/02

Witnessed, Read, and Understood by: John Murphy Date 5/24/02

Witnessed, Read, and Understood by: J. Hartog Date 5/24/02

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CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

- (8) equal contribution
- (9) Fixed abrasive polish, no polish slurry, different
polish steps
- (10) Invention will enable reduction of cost of ownership
Compared to Slurry.
- enables STI polish without requirement of excess slurry.
- enables STI polish with reduced step height budget required
for 143 nm lithography.

Inventor(s): William Wainright Date: 8/28/02Inventor(s): J. Edwards Date: 8/28/02Inventor(s): D. C. Loh Date: 8/28/02Witnessed, Read, and Understood by: R. J. Lewis Date: 8/28/02Witnessed, Read, and Understood by: R. J. Lewis Date: 8/28/02

Each page upon which information is entered should be signed and witnessed.



CYPRESS

STI Invention Disclosure

Option 1

- No Nitride LIM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

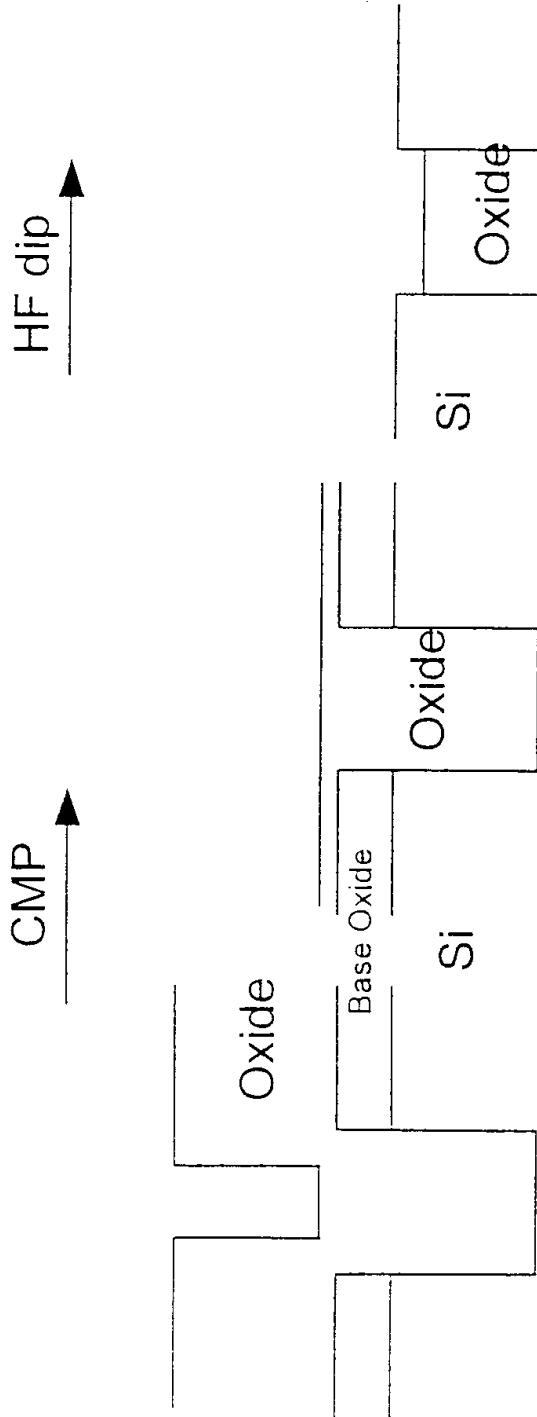


Exhibit A- page 8



STI Invention Disclosure

Method of Making STI

Option 1

WD#03	24-AUG-00 dense	WD#01	25-AUG-00
Depth 43nm		Depth 375nm	
10.0kV X80.0K		10.0kV X80.0K	
320.0nm		320.0nm	
*X : 000000		*D : 000000	

Exhibit A - page 9



CYPRESS

Option 2

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

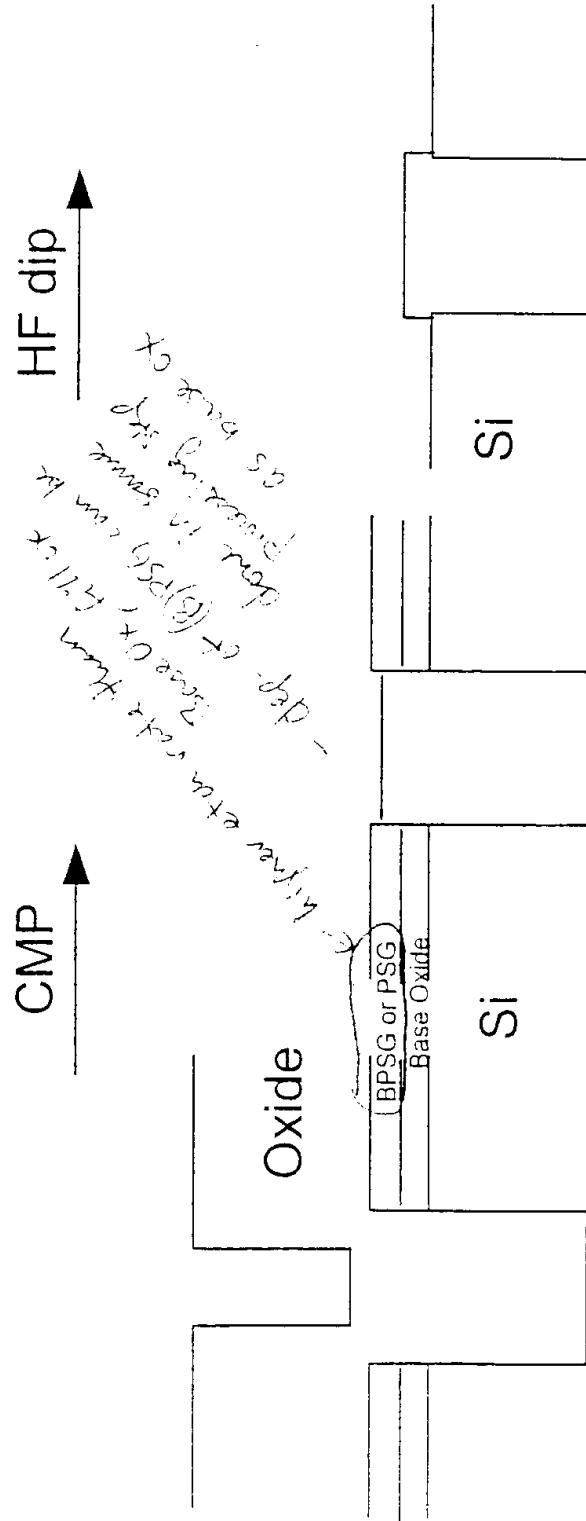


Exhibit A - page 10



Option 3

کمپانی سیپریس
Cypress Semiconductor Corporation

- Use thin Nitride
- polish to flatness - Fixed Abrasive, stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step height

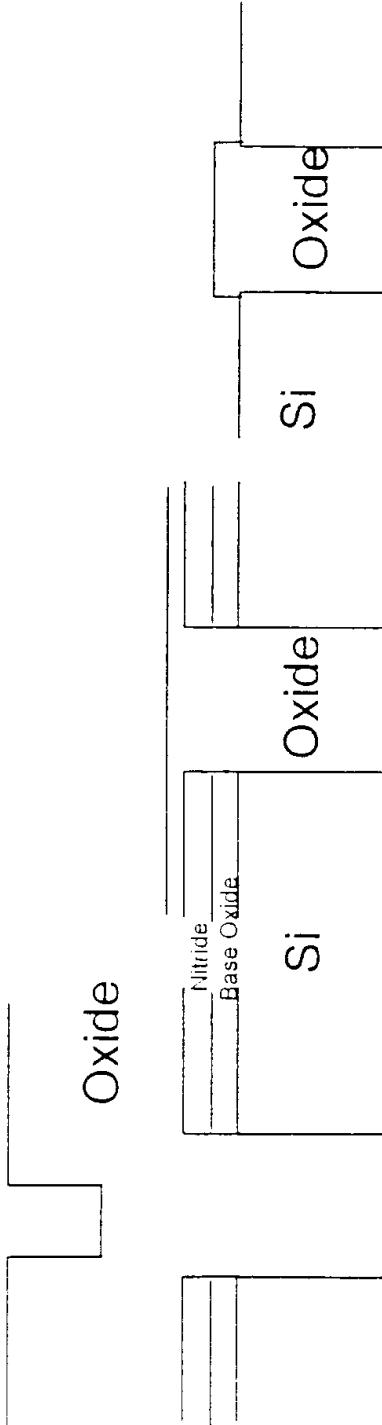
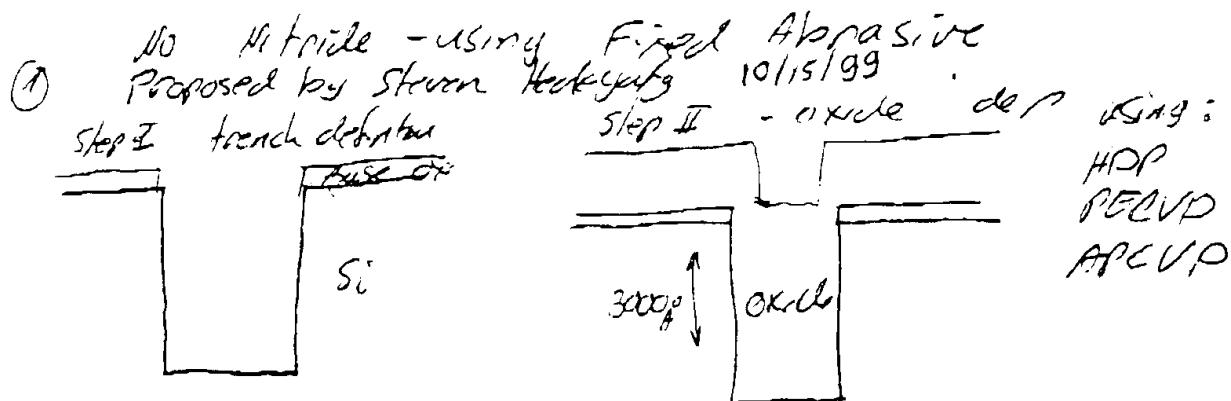


Exhibit A- page 11

STC

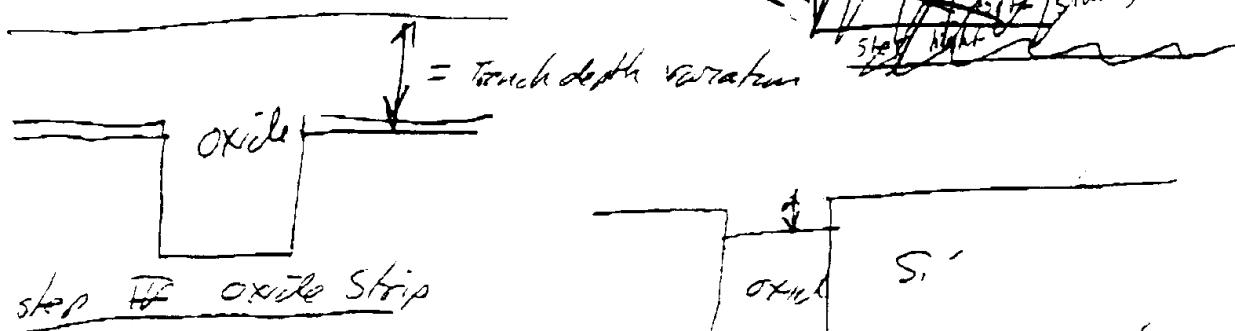
method of making shallow trench isolation
structure with no/ or thin nitride over stop.



in step II
need to deposit trench depth + trench depth variation

Step II Polish

due to Fixed Abrasive properties over will self planarize
once flatness is achieved.



Step III oxide Strip

strip will result in oxide below Si level

Steven Hegedusic, Ramkumar, Bill Katay, Mark Allard

S. Hegedusic
A. Blosie

10/15/99

10/15/99

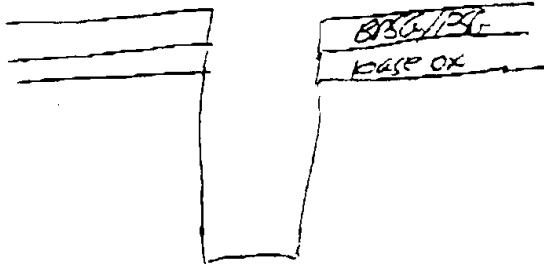
Exhibit B- page 1

570

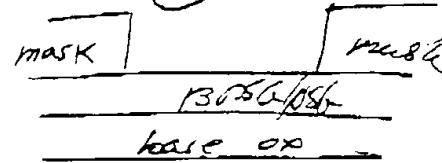
as long as trench depth variation is controlled below a certain number i.e. $\pm 500 \mu$ then polish can be done without ~~PSG~~ nitride layer.

(2) 2nd method use of PS/BSIG layer as a base oxide or on top of base oxide

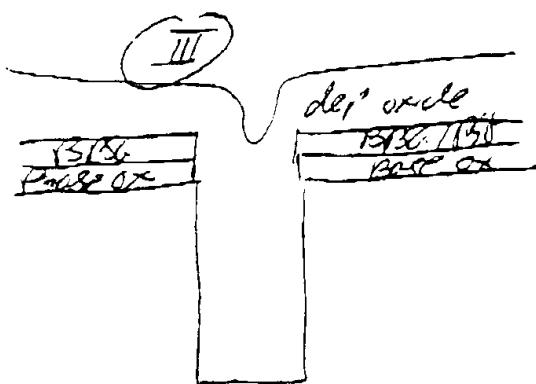
(II)



(I)

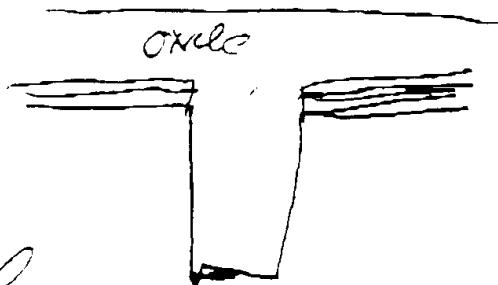


(III)



(III)

Polish using Fixed Abrasive



BSI Kouthey R.K. Jr

S. Hegdekar

Hans Block

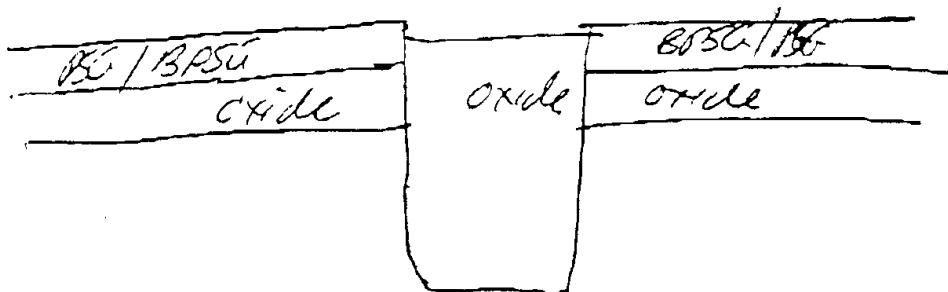
11/15/99

11/15/99

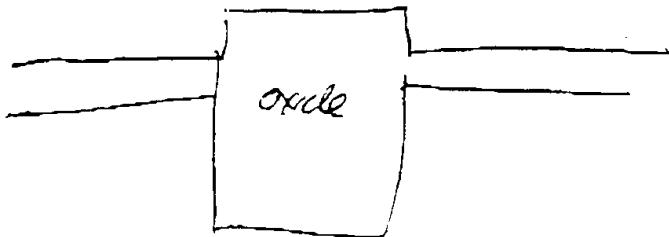
Exhibit B- page 2

~~strip oxide back to BOSE~~

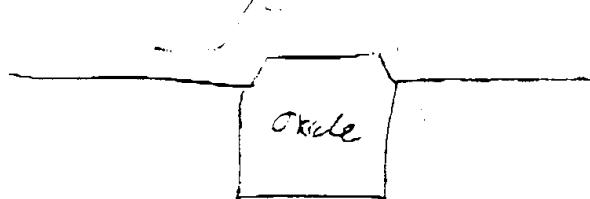
Polish Back to BOSE layer
strip



use wet strip BOSE ER is N 50 times
thermal oxide rate so result will be
after strip I



after strip II



BH Recovery 1/2k Cello

S. Hedges
Dk. 1/2k

11/15/89
11/16/89

Exhibit B - page 3

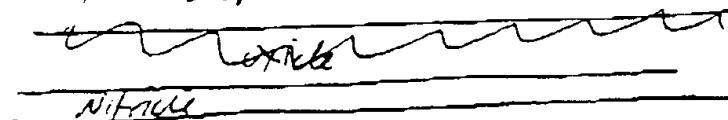
STC

(3)

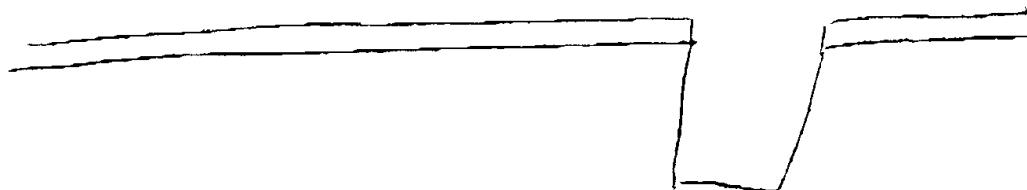
use thin Nitride for STC

Nitride is used only as a means
to determine oxide height above Si

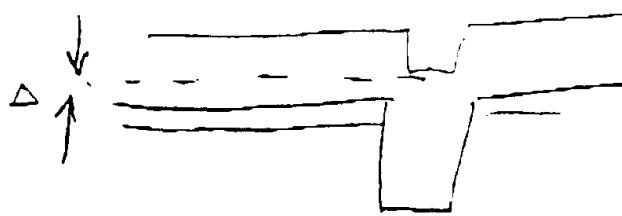
I dep thin Nitride



II mask and etch



III

dep HDP oxide or PECD oxide or APCVD
oxide

Thickness is
targeted to
achieve planarity
at D & above

Si

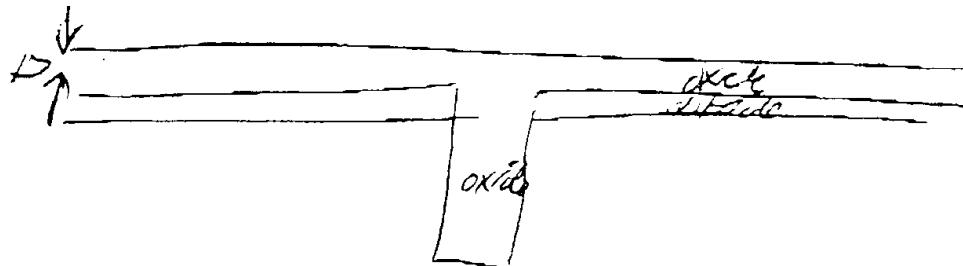
Bill Kaunney - 1/26/00
of Hedgehog
Alain Birose

11/15/99 -
11/15/99 -

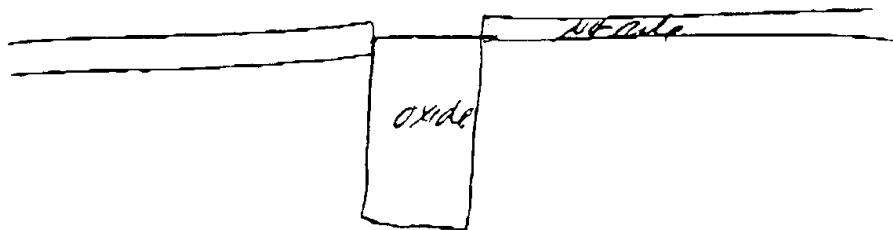
Exhibit B- page 4

~~FF~~

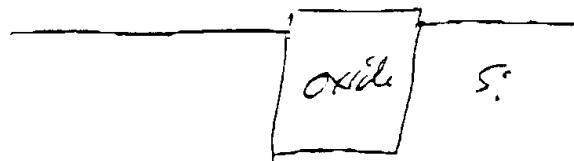
CMR



IV wet strip of oval



V nitrate strip



Bill Kowalsky 1/16/00

S. Hedley
Alvin Blane

10/15/99

10/15/99

Exhibit B - page 5



PATENT
5298-04700/PM100028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A
PLANARIZED SEMICONDUCTOR
STRUCTURE

Group Art Unit: 1763

Examiner: Goudreau, G.

Atty. Dkt. No.: 5298-04700

CERTIFICATE OF MAILING
37 C.F.R. § 1.18

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Steven Hedayati, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

 2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

RECEIVED

SEP 26

OFFICE OF PETITIONS

CONCEPTION

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Date: _____

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1. INVENTOR(S)

DISCLOSURE NO PM 00028A. Name YITZHAK GLICHT CY Initials Y.G. Empl. No. 7395 Ext. No. 2719Citizenship U.S.A. Dept # SCP Home Phone No. 408-253-2827Home Mailing Address 1761 HERON DR. SCOTTSDALE, AZ 85257B. Name William Hartley CY Initials B/H Empl. No. 135 Ext. No. 2673Citizenship U.S. Dept # Home Phone No. 408-247-0551Home Mailing Address 7555 Homestead #45 San Jose, CA 95051
2155 Homestead #5
95051C. Name Steven Healyati CY Initials S.H. Empl. No. 8584 Ext. No. 4556Citizenship U.S. Dept # 31C8 Home Phone No. 408-927-0187Home Mailing Address 1240 Valley Quail Circle San Jose CA 951202. TITLE OF INVENTION Method of making shallow trench isolation Structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings RedactedWhere can first drawing be found RedactedB. Date of first written description RedactedWhere is description found RedactedC. Date of first oral disclosure to others RedactedTo whom? Discussed with KTL, SS, I, B/K

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Inventor(s) Yitzhak Glicht Date 3/24/00Inventor(s) William Hartley Date 3/24/00Inventor(s) Steven Healyati Date 3/24/00Witnessed, Read, and Understood by: T. Tipton Date 3/24/00Witnessed, Read, and Understood by: J. Soddy Date 3/24/00

(Each page upon which information is entered should be signed and witnessed.)

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1. INVENTOR(S)

DISCLOSURE NO. _____

A. Name Kankumar CY Initials KTR Empl. No. 3305 Ext. No. 2720
Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031
Home Mailing Address 1193 LYNBROOK WAY ; SAN JOSE ; CA 95129

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

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Inventor(s) _____ Date _____

Inventors: _____ Date: _____

Witnessed, Read, and Understood by _____ Date _____

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Exhibit A- page 2

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CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. TEST OF DEVICE

- A. Date: _____ Witness(es): _____
B. Results: _____

6. SALE

- A. Was invention sold or offered for sale? Yes No ✓
B. Was invention used to make, assemble or test a commercial product? Yes No ✓
C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes No ✓
D. Actual or estimated date of first sale, offer or commercial use _____
E. Is invention part of a product for which there is a data sheet? Yes No ✓ (If yes, attach a copy)
F. Actual or estimated date of publication, release or availability of data sheet _____

7. USE

- A. Is invention presently being used? Yes No ✓

- B. In what product or process is invention presently being used?

Are there specific plans for its use in near future? In what products or processes?

RAM-X

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS

5,972,792 / 4010573 and 5,782,675 / 5,919,072

4,393,627 / 5,311,520

9. WAS INVENTION Conceived (Yes (No) Constructed (Yes (No) Tested (Yes (No) during performance of Government Contract?

Contract Number _____

(Give Full Contract Number)

=====

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s) Date

Inventor(s) Date

Inventor(s) Date

Witnessed, Read, and Understood by: Date

Witnessed, Read, and Understood by: Date

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 3

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method
5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

1. The purpose of the invention is to improve the manufactureability of Si and reduce cost. This is done by reducing processing steps.

2. Current technology (AT-1.8 TDI) calls for the following steps:

1. Pre-Layout (FAB 1, STATE 1, STEP 1, LAYER 1, FILM 1, LAYER 1)
2. Pre-Layout (FAB 1, STATE 1, STEP 1, LAYER 1, FILM 1, LAYER 1)
3. Pre-Layout (FAB 1, STATE 1, STEP 1, LAYER 1, FILM 1, LAYER 1)

Inventor(s) M. Sadiq Date 8/24/00

Inventor(s) J. Horowitz Date 8/24/00

Inventor(s) D. H. J. P. Date 8/24/00

Witnessed, Read, and Understood by: M. Sadiq Date 8/24/00

Witnessed, Read, and Understood by: M. Sadiq Date 8/24/00
Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3) Disadvantages addressed by invention:

1. thick nitride layer required to overcome severe diffusion in siliciding caps process. This makes new failure stress effects.
2. additional etch required to Etch nitride
3. extra step after etch step which can result in Poly stripes
4. twice etch followed by an extra step released by nitride.

(4) The current invention has three options of using

First abrasive polish as the ~~nitride~~ mask or polish.

The main advantage of first abrasive is the negligible dielectric constant of nitride compared to conventional dry etch processes.

The second advantage is soft plasma etch which reduces surface roughness.

Option I - no nitride hard mask

In this option it is vital that after Film deposition on base and trench sidewall, a 2nd step is when the trench is opened. After trench open up it is crucial not to trench and cross the bottom of the trench + the trench sidewall orientation. After oxide deposition the oxide is polished off by first plasma to a residual thickness of c-500 Å. The last 4 steps are as follows and the sequence is as follows. The last two steps are optional and may be omitted.

Inventor(s):	<u>Munish Rathy</u>	Date:	<u>1/26/01</u>
Inventor(s):	<u>A. V. Singh</u>	Date:	<u>1/26/01</u>
Inventor(s):	<u>J. S. Gopalan</u>	Date:	<u>1/26/01</u>
Witnessed Read and Understood by:	<u>M. Rathy</u>	Date:	<u>1/26/01</u>
Witnessed Read and Understood by:	<u>A. V. Singh</u>	Date:	<u>1/26/01</u>

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Deposit Thin Nitride -

grow base oxide grow thin layer of nitride (0.500 μ)
expose first oxide mask fresh trench, deposit nitride
polish down to ~~nitride~~ step on oxide at a predetermined
residual oxide when no nitride. Step remaining oxide
Step remaining nitride.

Option III

grow base oxide deposit BPSG, expose first
etch trench, deposit nitride, which is BPSG/nitride layer
use wet steps to remove remaining BPSG, and etch first
nitride step to remove nitride, use to wet Etch BPSG
BPSG is removed to nitride layer then etch with
nitride + positive type of nitridation mask 5 μ .

- ⑥ - This invention and all improvements of this disclosure
claiming the use of nitride as a nitridation mask
⑦ - Invention is made fully by the person named, except for
their power to assign to another, after:

Inventor(s) John M. Murphy, Date 3/24/81

Inventor(s) J. H. Sizelove, Date 3/24/81

Inventor(s) J. H. Sizelove, Date 3/24/81

Witnessed, Read, and Understood by: J. H. Sizelove, Date 3/24/81

Witnessed, Read, and Understood by: J. H. Sizelove, Date 3/24/81

(Each page upon which information is entered should be signed and witnessed.)

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM
(INSERT ADDITIONAL INFORMATION)

- (8) equal contribution
- (9) Fixed Abrasive polish, no polish steps, different
polish steps
- (10) Invention will enable reduction of cost of ownership
Corporated to Slurry.
- enable STI polish without requirement of 20-50 mesh
- enable STI polish with reduced step height budget required
for 193 nm lithography.

inventor(s)	<u>William Mawling</u>	Date	<u>6/26/02</u>
inventor(s)	<u>J. Hedges</u>	Date	<u>6/26/02</u>
inventor(s)	<u>J. C. L. Li</u>	Date	<u>6/26/02</u>
Witnessed, Read, and Understood by:	<u>E. S. Doherty</u>	Date	<u>6/26/02</u>
Witnessed, Read, and Understood by:	<u>E. S. Doherty</u>	Date	<u>6/26/02</u>

(Each page upon which information is entered should be signed and witnessed.)



Option 1

- No Nitride HM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

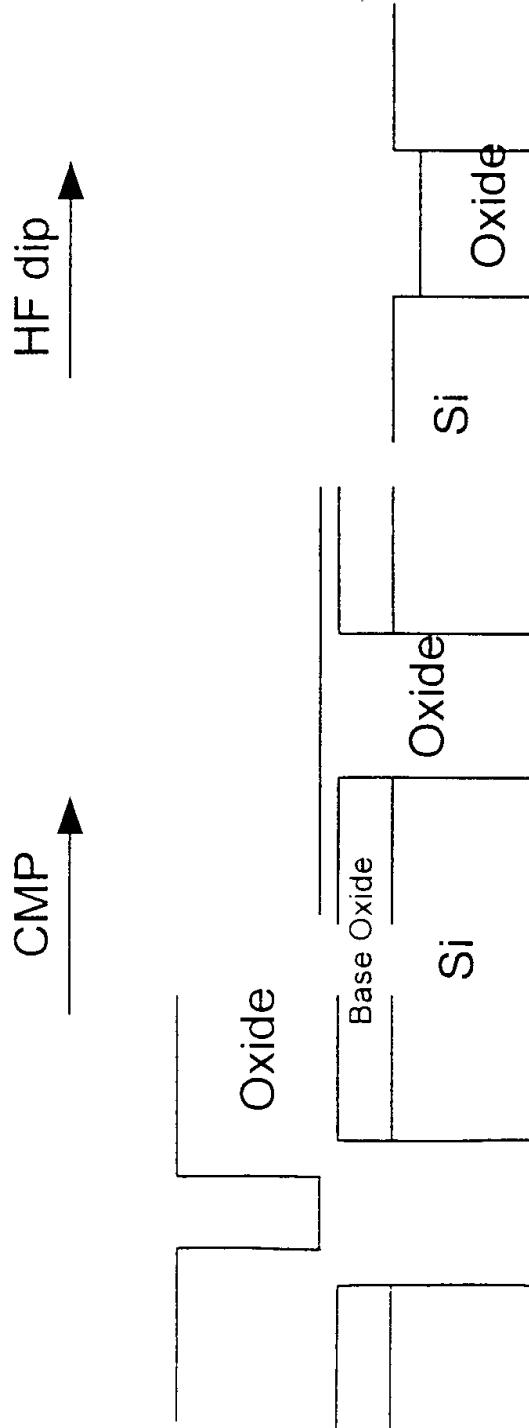


Exhibit A- page 8



CYPRESS

STI Invention Disclosure

Method of Making STI

Option 1

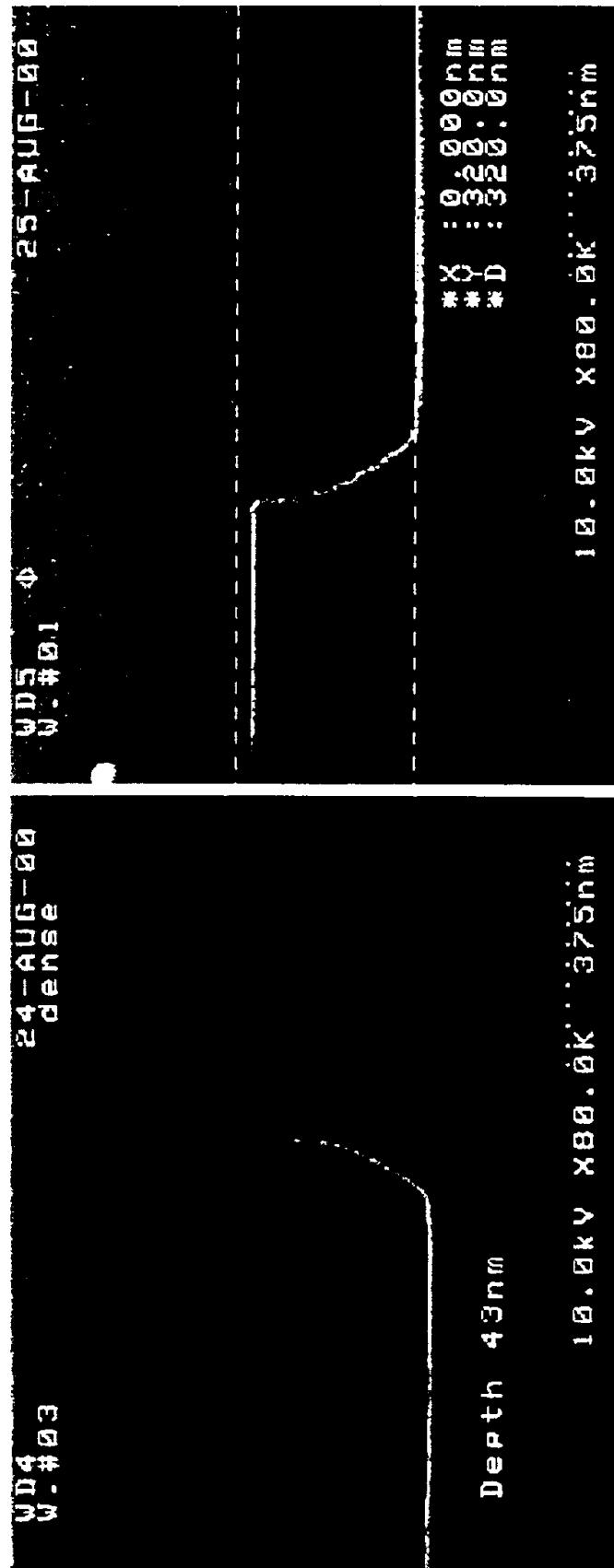


Exhibit A - page 9



Option 2

- Use doped oxide to increase selectivity during wet Dip polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

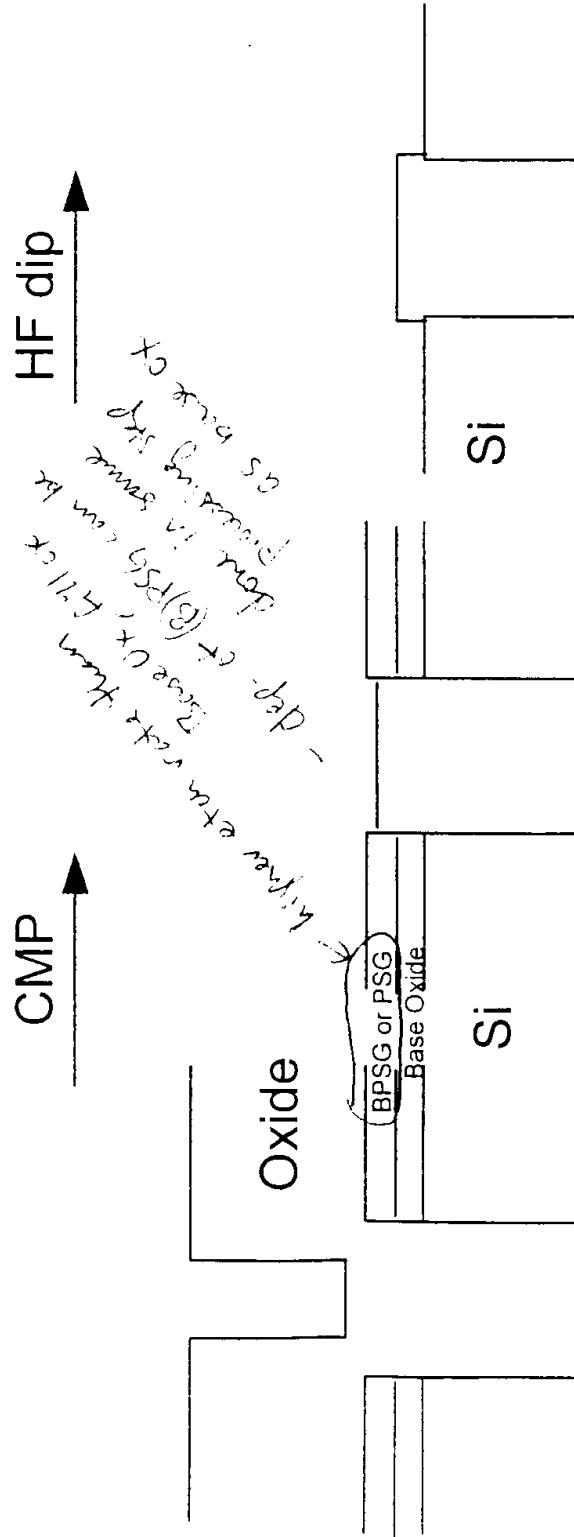


Exhibit A - page 10



CYPRESS

STI Invention Disclosure

Option 3

↓ ↓ Nitride (2000 Å) to
↓ ↓ CMP to CVD Silicon Oxide

- Use thin Nitride
- polish to flatness - Fixed Abrasive ,stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step hieght

CMP →

HF dip + Nitride Strip →

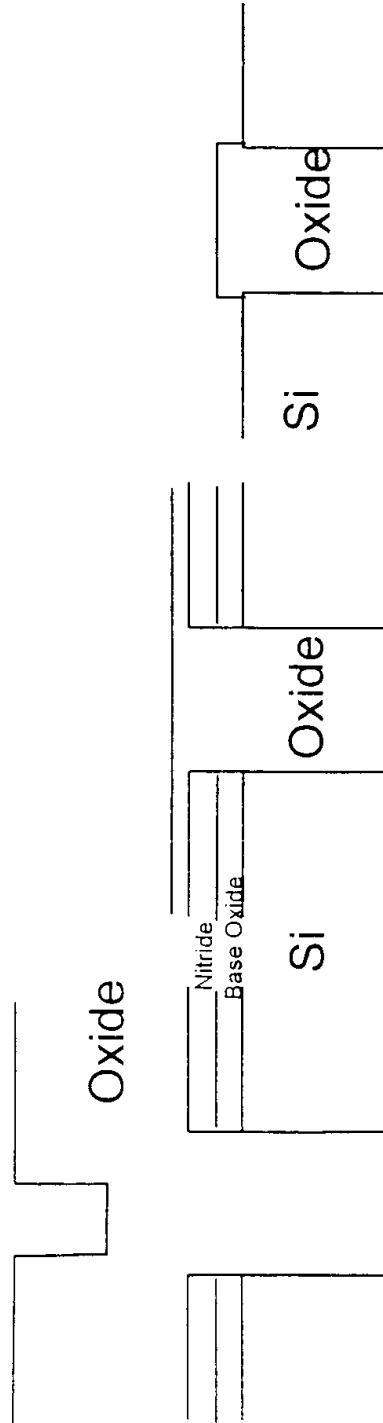
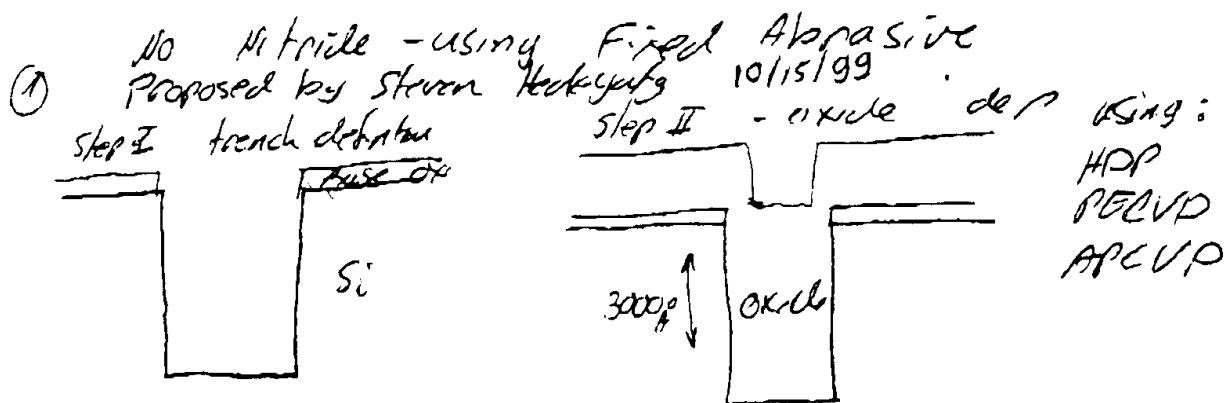


Exhibit A- page 11

STC

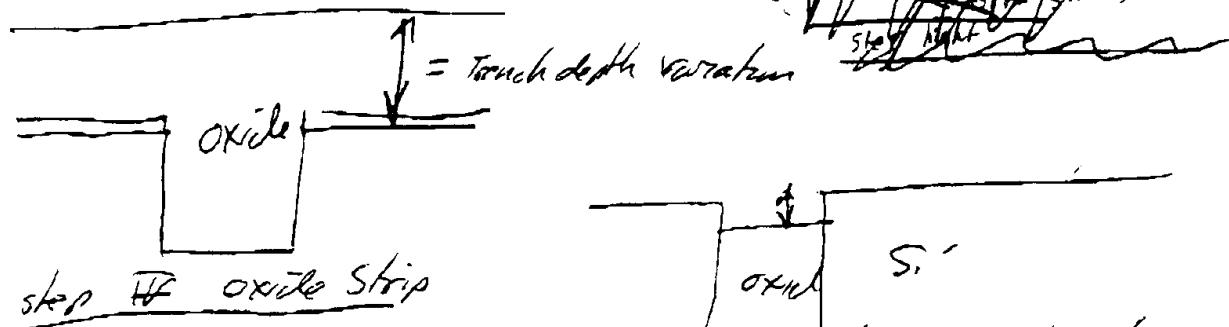
method of making shallow trench isolation
structure with no/or thin nitride over stop.



in step II
need to deposit trench depth + trench depth variation

Step II Polish

due to Fixed Abrasive properties over will self planarize
once flatness is achieved.



strip will result in oxide below Si level

Steven Hegedusic, Ram Kumar, Bill Katay, Kirk Gibson

S. Hegedusic
F. Blosse

10/15/99

10/15/99

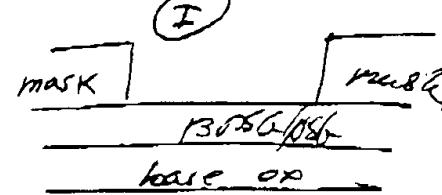
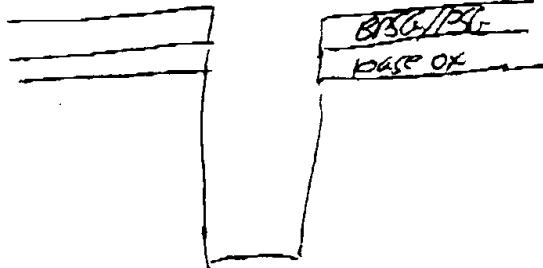
Exhibit B- page 1

STC

as long as trench depth variations are controlled below a certain number ie \pm 500 Å then polish can be done without ~~the~~ nitride layer.

(2) ^{2nd} Method use of PS/BPSG layer as a base oxide or on top of base oxide

(II)



del oxide

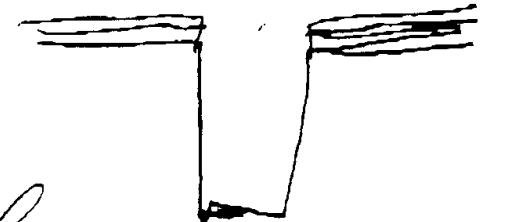
BPSG/BPSG

base ox

(III)

Polish using Fixed
Abrasive

oxide



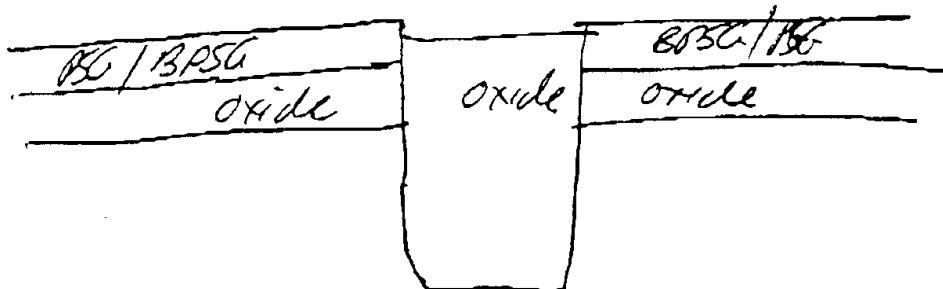
BII Kouthey R.K Jr
S. Hedyali
Alan Blase

11/15/99
11/15/99

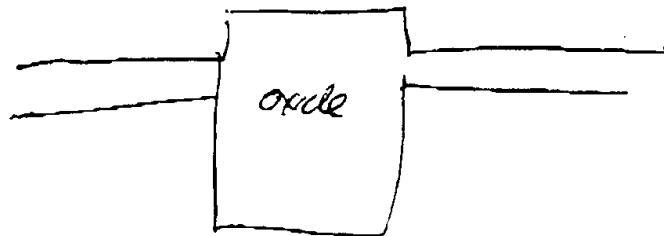
Exhibit B- page 2

~~strip oxide back to BPSG~~

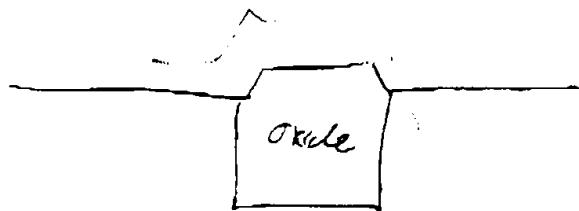
Polish Back to BPSG layer
strip



use wet strip BPSG ER is N 50 times
thermal oxide rate so result will be
after strip I



after strip II



BII Kourney 1/3, b Ciba

S. Hedges
Dk. - 1/22

11/15/89
11/15/90

Exhibit B- page 3

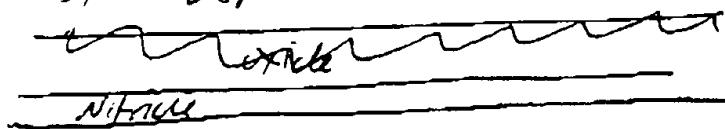
STC

(3)

use thin Nitride for STC

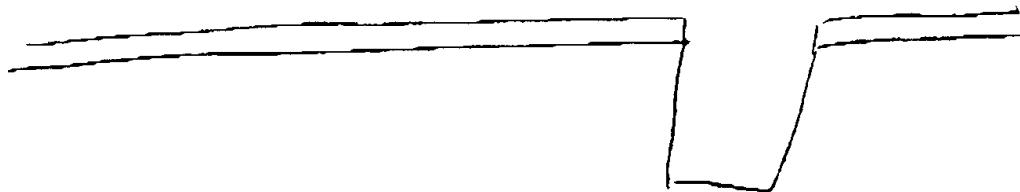
Nitride is used only as a means
to determine oxide height above Si

It dep their Nitride

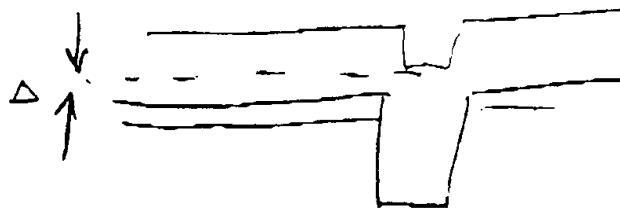


II

mask and etch



III

dep HfP oxide or PEVCO oxide or APCVD
Oxide

Thickness is
targeted to
achieve planarity
at D & above

Si

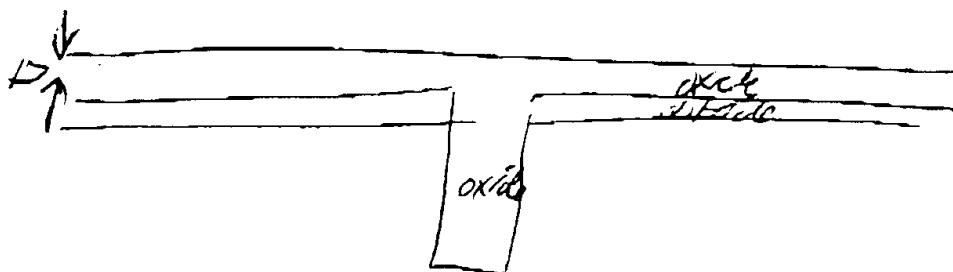
Bill Courtney - 16k fm

S. Hedges
Alain Blouin11/15/99
11/15/99

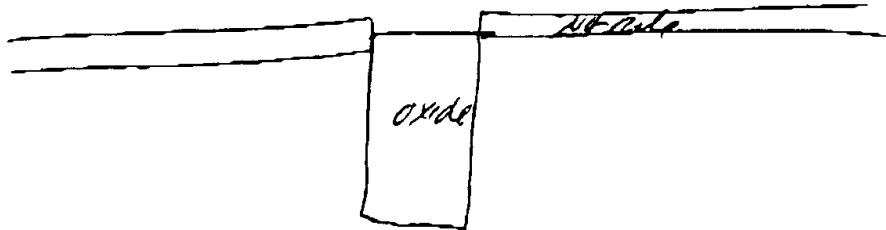
Exhibit B- page 4

~~FF~~

CMR



II wet strip of oxid



III nitrate strip



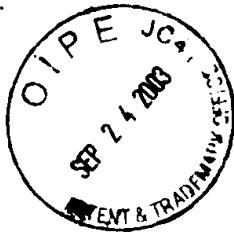
B71 Kowzey 1/16 bilader

S. Hedges
Hawai Blm

11/15/99

11/15/99

Exhibit B- page 5



RECEIVED
SEP 30 2003
TC 1700

PATENT
5298-04700/PM00028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

§ Group Art Unit: 1763

§ Examiner: Goudreau, G.

§ Atty. Dkt. No.: 5298-04700

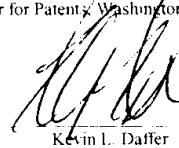
Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A
PLANARIZED SEMICONDUCTOR
STRUCTURE

CERTIFICATE OF MAILING
37 C.F.R. § 1.18
I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03
Date



Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Krishnaswamy Ramkumar, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

RECEIVED

SEP 26 2003

OFFICE OF PETITIONS

CONCEPTION

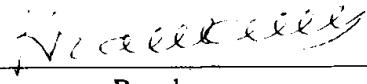
3. As supported below, I, along with Yitzhak Gilboa, William W.C. Koutny, Jr. and Steven Hedayati, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.
4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.
5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.
6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.
7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.


Krishnaswamy Ramkumar

Date: 11/14/03

CONLEY ROSE, P.C.

INTELLECTUAL PROPERTY LAW
INCLUDING
PATENTS, TRADEMARKS,
COPYRIGHTS AND
UNFAIR COMPETITION

A PROFESSIONAL CORPORATION
THE CHASE BUILDING
700 LAVACA, SUITE 720
AUSTIN, TEXAS 78701-3108
(512) 476-1400
FACSIMILE (512) 703-1250
www.conley-rose.com

HOUSTON OFFICE
CHASE TOWER
600 TRAVIS, SUITE 7100
HOUSTON, TEXAS 77002-2912
(713) 238-8000
FACSIMILE (713) 238-8008

KEVIN L. DAFFER
(512) 476-1400
kdaffer@conley-rose.com

5298-04700

August 21, 2003

Steven Hedayati
1240 Valley Quail Circle
San Jose, CA 95120

Via Certified Mail, RRR

Re: Declaration to Predate Reference with Regard to Cypress Patent Application PM00028

Dear Mr. Hedayati:

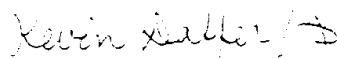
I am contacting you in regard to a patent application filed on behalf of Cypress Semiconductor Corporation. You are listed as a co-inventor of the invention, along with Yitzhak Gilboa, Krishnaswamy Ramkumar and William W. C. Koutny, Jr. The application is entitled "Method of Making a Planarized Semiconductor Substrate" and Cypress's reference number is PM00028. The application was filed on April 30, 2001.

We have received a rejection from the U.S. Patent and Trademark Office citing some patents and publications which teach some of the limitations claimed in the patent application. One of the references may be overcome by filing a declaration that the conception date of the invention is prior to the publication date of the cited reference. Enclosed herein is a copy of such a declaration. Please review, sign and return the enclosed declaration as soon as possible. Your immediate attention to this matter is appreciated.

I have also attached a copy of the invention disclosure form and copies of Yitzhak's lab notebook pertaining to the patent application. The documents will be filed with the declarations as Exhibits A and B, respectively. As noted in the declarations, the reference we are declaring to predate is an article in *Solid State Technology* entitled "Improved Planarization for STI with Fixed Abrasive Technology" by Vo et al., which was published in June of 2000. If you would like me to send you a copy of the article, please let me know.

Please do not hesitate to call me at (512) 703-1242 if you have any questions.

Very truly yours,



Kevin L. Daffer

RECEIVED

Enclosure

SEP 2 8

OFFICE OF PETITIONS

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO. PM 00028A. Name Yitzhak Gersh CY Initials YG Empl. No. 7295 Ext. No. 2719Citizenship U.S.A. Dept # 208 Home Phone No. 408-253-2827Home Mailing Address 1761 HERCULANEUM SEMICONDUCTOR CIR 95027B. Name William Bentley CY Initials WB Empl. No. 135 Ext. No. 2633Citizenship U.S. Dept # 3108 Home Phone No. 408-247-6255Home Mailing Address 2555 Homestead #45 San Jose CA 95131
2075 Homestead 45 95051C. Name Steven Healyati CY Initials SJH Empl. No. 8534 Ext. No. 4556Citizenship US Dept # 3108 Home Phone No. 408-927-0187Home Mailing Address 1240 Valley Quail Circle San Jose CA 951202. TITLE OF INVENTION Method of making Shallow trench isolation Structure

3. CONCEPTION OF INVENTION

A. Date of first drawing or drawings Redacted
Where can first drawing be found RedactedB. Date of first written description Redacted
Where is description found RedactedC. Date of first oral disclosure to others Redacted
To whom? Discussed with KTR 5511 1315

4. CONSTRUCTION OF DEVICE

A. Date Completed _____

B. Was prototype made? _____

C. By whom made? _____

D. Where can the prototype be found? _____

Inventor(s) Yitzhak Gersh Date 3/24/00Inventor(s) William Bentley Date 3/24/00Inventor(s) Steven Healyati Date 3/24/00Witnessed, Read, and Understood by T. Parker Date 3/24/00Witnessed, Read, and Understood by U. Sader Date 3/24/00

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO. _____

A. Name Ramkumar CY Initials KTR Empl. No. 3305 Ext. No. 2720
Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031
Home Mailing Address 1193 LYNBROOK WAY ; SAN JOSE ; CA 95128

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
Citizenship _____ Dept # _____ Home Phone No. _____
Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

- A. Date of first drawing or drawings _____
Where can first drawing be found _____
- B. Date of first written description _____
Where is description found _____
- C. Date of first oral disclosure to others _____
To whom? _____

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Inventor(s): _____ Date: _____

Inventor(s): _____ Date: _____

Inventor(s): _____ Date: _____

Witnessed: Read and Understood by: _____ Date: _____

Witnessed: Read and Understood by: _____ Date: _____
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Exhibit A- page 2

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

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C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes No
D. Actual or estimated date of first sale, offer or commercial use _____
E. Is invention part of a product for which there is a data sheet? Yes No ✓ (If yes, attach a copy)
F. Actual or estimated date of publication, release or availability of data sheet _____

7. USE

- A. Is invention presently being used? Yes No ✓

- B. In what product or process is invention presently being used?

Are there specific plans for its use in near future? In what products or processes?

RAY-D

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS

5,972,792 / 4010523 and 5,782,675 / 5,919,072
4,393,627 / 5,782,675

9. WAS INVENTION Conceived (Yes (No ✓) Constructed (Yes (No ✓) Tested (Yes (No ✓) during performance of Government Contract?

Contract Number _____
(Give Full Contract Number)

=====

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s): Walter M. Kelly Date: 5/22/00

Inventor(s): J. Michael J. Kelly Date: 5/22/00

Inventor(s): J. Michael J. Kelly Date: 5/22/00

Witnessed: Read and Understood by: Walter M. Kelly Date: 5/22/00

Witnessed: Read and Understood by: Walter M. Kelly Date: 5/22/00

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

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4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
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6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, by a single step reducing processing steps.
2. Current technology (LTO-102 TDS) calls for the following steps:

Step 1: Deposit Si_3N_4 , SiO_2 , Ti-SiO_2 & TiO_2 on Si .
Step 2: H_2O_2 etch Si_3N_4 & SiO_2 to form TiO_2 & Ti-SiO_2 .
Step 3: H_2O_2 etch TiO_2 & Ti-SiO_2 to form TiO_2 & Ti-SiO_2 .

Inventor(s): William Brady Date: 8/24/00

Inventor(s): J. Daniel Date: 8/24/00

Inventor(s): L. H. J. Date: 8/24/00

Witnessed, Read, and Understood by: John D. Sodish Date: 8/24/00

Witnessed, Read, and Understood by: John D. Sodish Date: 8/24/00

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 4

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3) Disadvantages addressed by invention:

1. Thick silicon-layer required to overcome total etching in plasma step. This results in higher stress effects.
2. Anisotropic etch required to Etch wafer.
3. Extra steps after whole steps which can result in Poly stringing.
4. Tungsten acid film deposition to overcome steps induced by nitride.

(4) The current invention has three options of using TiCat Plasma polish as the ~~main~~ method of polish.

The main advantage of TiCat Plasma is the negligible amount of Etched compared to conventional plasma process.

The second advantage is self planarization, no extra recesses at all.

Option I - No Nitride Hard mask:
 In this option we obtain the usual TiCat pattern on base and trench each composed of one step up followed by trench or option. After trench each side of the trench in the trench and across the thickness of thickness of the hard + trench depth variation. After each step up the next is performed
 using TiCat Plasma to a planned thickness of 0-500 Å.
 The last two steps of a not planned by the process the last two steps of the process to remove the recessed area.

Inventor(s) Manish Bhatia Date 3/26/02

Inventor(s) J. S. Kothiyal Date 3/26/02

Inventor(s) R. P. Patel Date 3/26/02

Witnessed, Read, and Understood by: Manish Bhatia Date 3/26/02

Witnessed, Read, and Understood by: A. K. Patel Date 3/26/02
 Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Resists This Article -

Start base oxide grow thin layer of nitrid (3-500Å)
 Expose full oxide mask, Etch trench, Deposit silicon oxide
 polish down to ~~the~~ stop on oxide at a predetermined
 thickness oxide above the etched. Stop remaining oxide.
 Stop Remaining Nitrid.

Option III

Start base oxide deposit EPOXY, expose and
 Etch trench, deposit silicon oxide, which is EPOXY/SILICON OXIDE
 Use wet stop to remove remaining EPOXY, use etching
 wet stop to remove oxide, Due to wet Etch Rate
 difference of Epoxy to oxide equal each other 2000
 Angstroms, no machine stops at nitrided, only, because of

- ⑥ To my knowledge of anyone's knowledge or other knowledge
 following the use of this article there shall be no
 damages to the company and/or to me for any damage or
 loss from this article to your company or myself.
- ⑦

Inventor(s) John M. Murphy Date 3/24/02

Inventor(s) J. Rodriguez Date 3/24/02

Inventor(s) J. Rodriguez Date 3/24/02

Witnessed, Read, and Understood by: John M. Murphy Date 3/24/02

Witnessed, Read, and Understood by: John M. Murphy Date 3/24/02
 Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

- (8) equal contribution
- (9) Fixed Abrasive polish, no polish steps, Different Polish Steps
- (10) - Invention will enable reduction of cost of ownership
Compared to Slurry.
- enables STC polish without segmentation of new slurry wash.
- enables STC polish with reduced step height budget required
for 125 nm lithography.

Inventor(s):	<u>Milton M. Hartung</u>	Date:	<u>2-25-90</u>
Inventor(s):	<u>E. L. Goss</u>	Date:	<u>2-25-90</u>
Inventor(s):	<u>J. C. Lai</u>	Date:	<u>2-25-90</u>
Witnessed, Read and Understood by:	<u>John Hartung</u>	Date:	<u>2-25-90</u>
Witnessed, Read and Understood by:	<u>E. L. Goss</u>	Date:	<u>2-25-90</u>

Each page upon which information is entered should be signed and witnessed.)



Option 1

- No Nitride LIM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

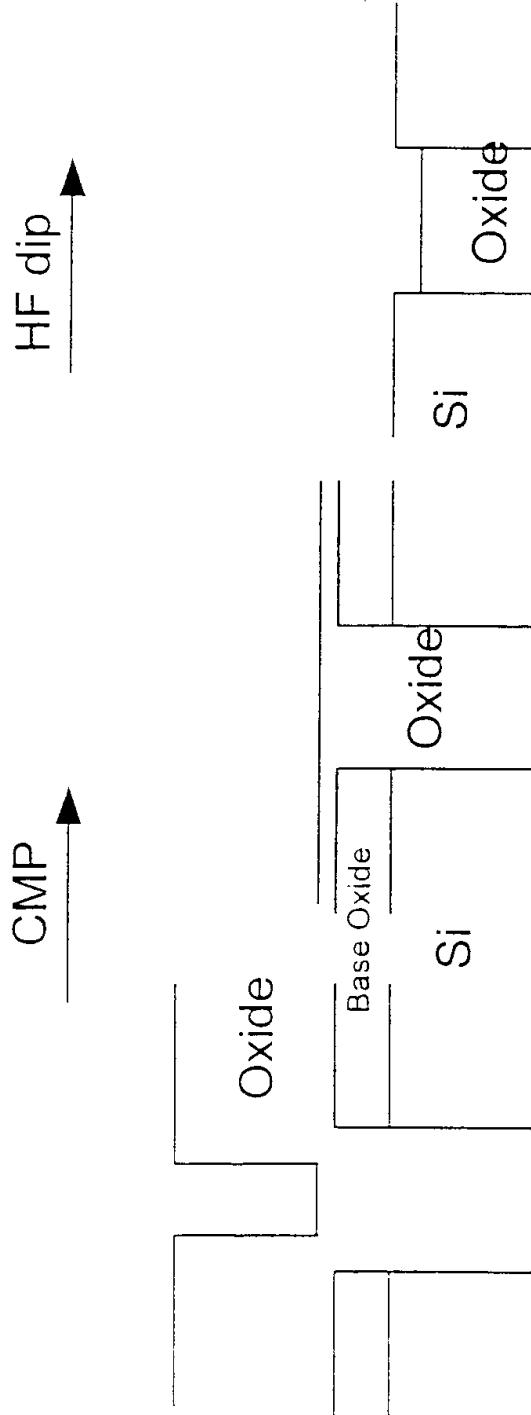


Exhibit A - page 8



STI Invention Disclosure

Method of Making STI

Option 1

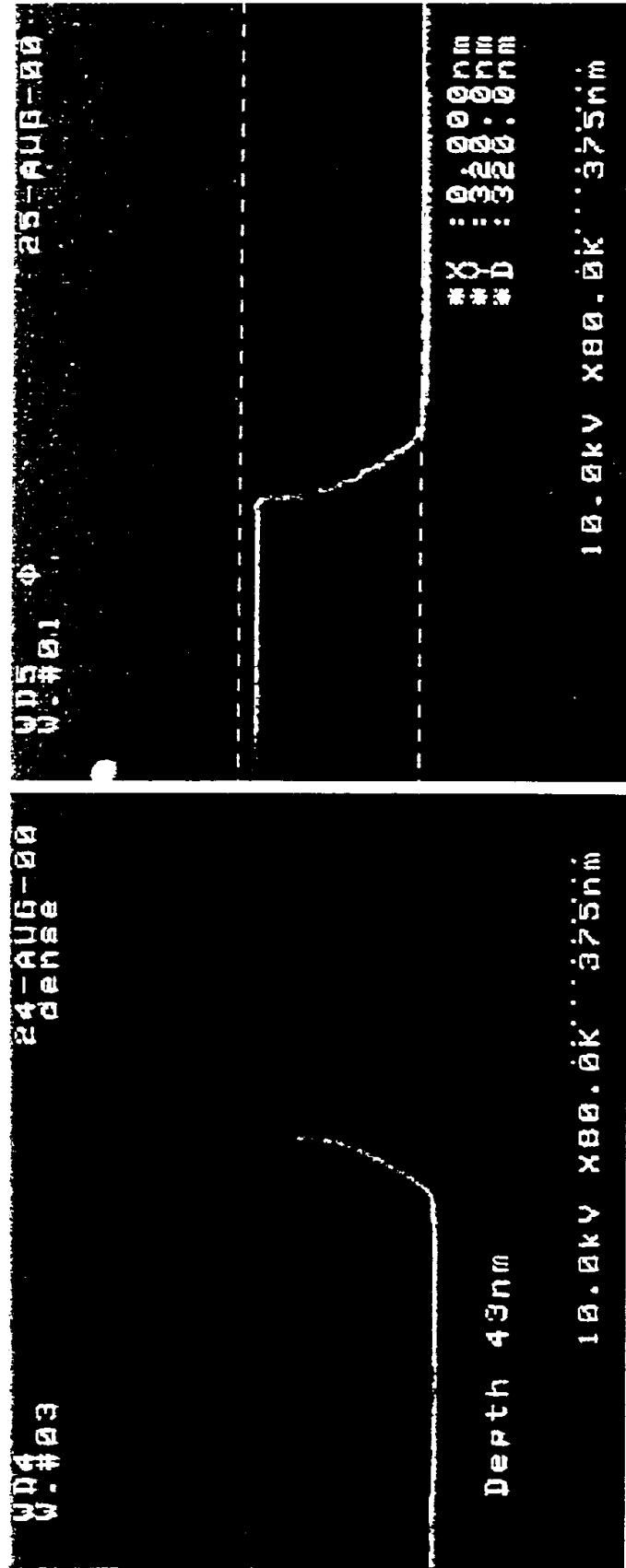


Exhibit A- page 9



CYPRESS

Option 2

- Use doped oxide to increase selectivity during wet Dip polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

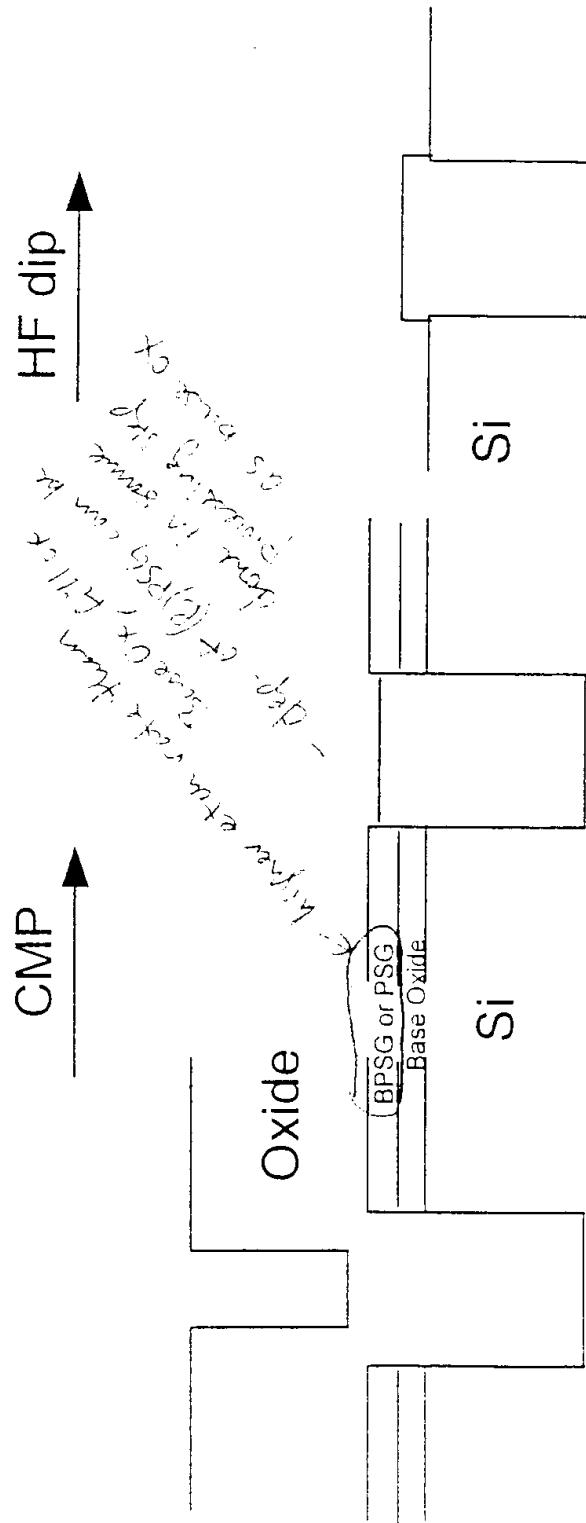


Exhibit A - page 10



Option 3

Use thin Nitride (~200 Å) to
determine step height
CMP to

- Use thin Nitride
- polish to flatness - Fixed Abrasive ,stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step height

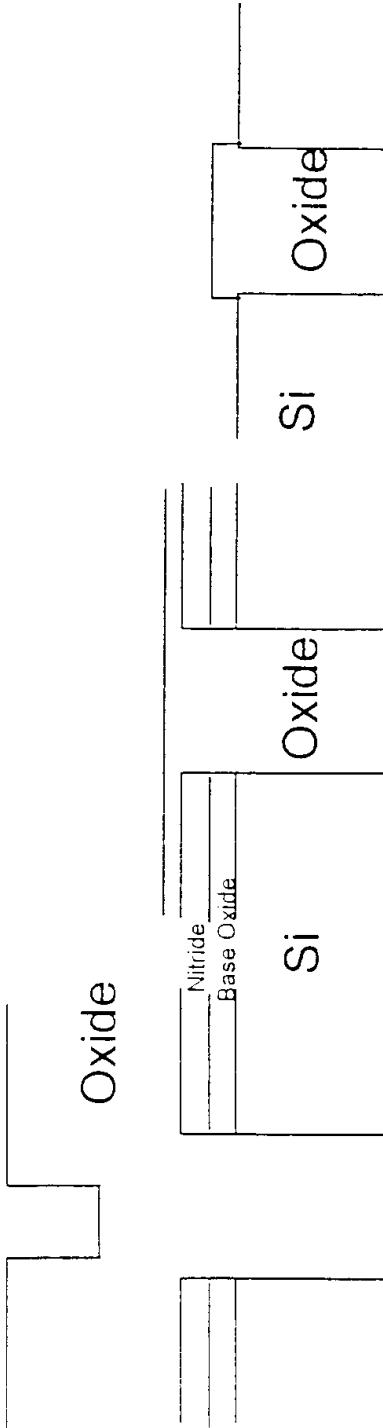
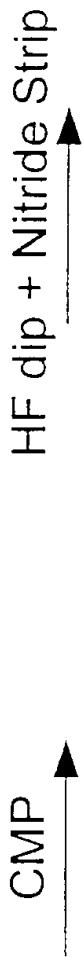
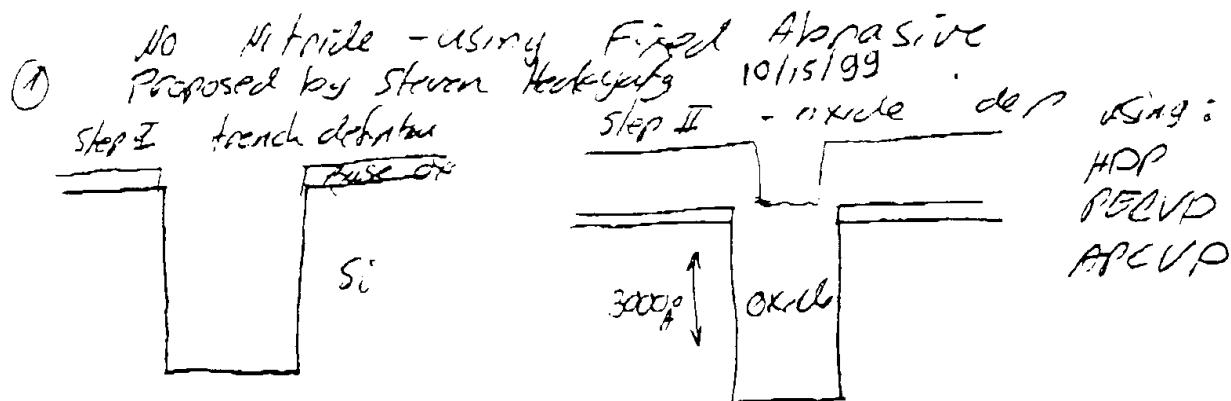


Exhibit A- page 11

STC

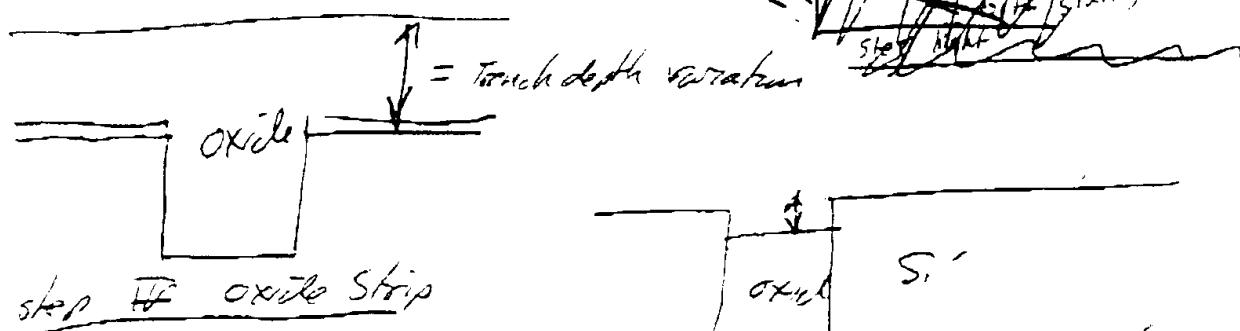
method of making shallow trench isolation
structure with no/or thin nitride CUR stop.



in step II
need to deposit trench depth + trench depth variation

Step II Polish

due to Fixed Abrasive properties CUR will self planarize
once flatness is achieved.



Step will result in oxide below Si level

Steven Hegedusic, Ramkumar, Bill Katay, Mike Allen

S. Hegedusic
A. Prostie

11/15/99
11/15/99

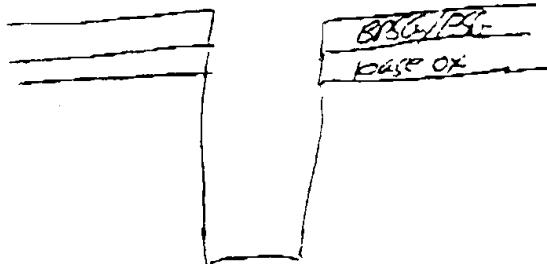
Exhibit B - page 1

SIC

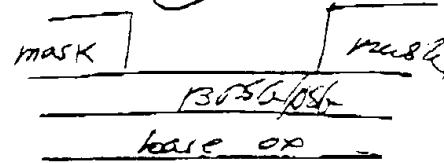
as long as trench depth variation is controlled below a certain number ie $\pm 500 \mu$ then polish can be done without ~~any~~ nitride layer.

(2) ^{2nd} method use of PS/BPSG layer as a base oxide or on top of base oxide

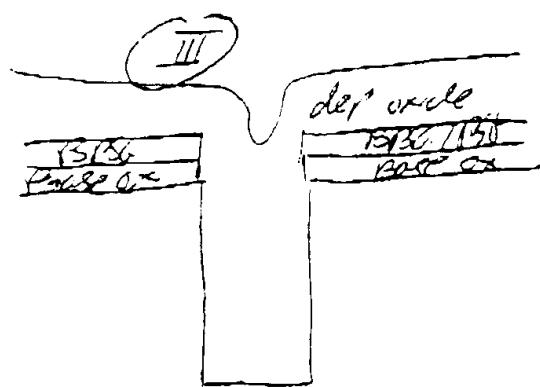
(II)



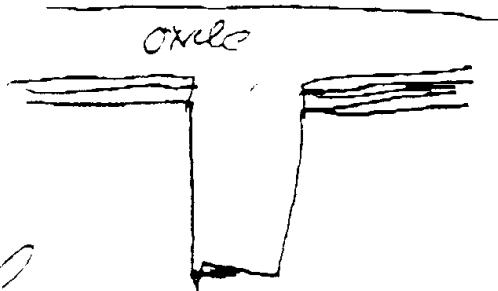
(I)



(III)



Polish using Fixed Abrasive



BII Kauthay R.K. Jr

S. Hedges
Hans Blox

11/15/89

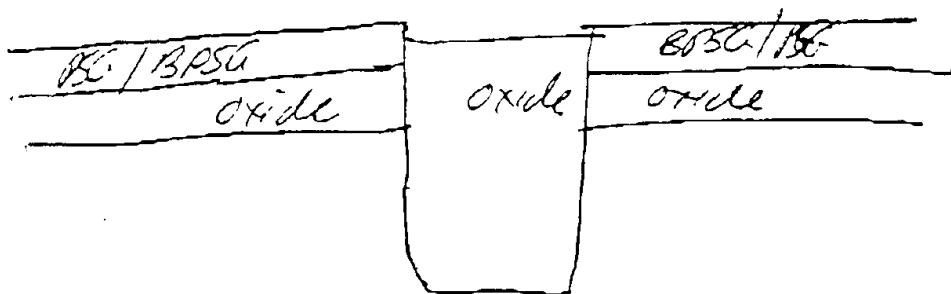
11/15/89

Exhibit B- page 2

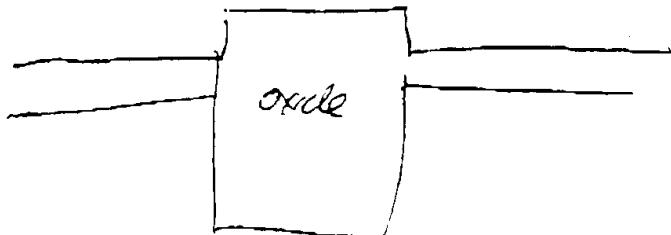
3

~~strip oxide back to BPSG~~

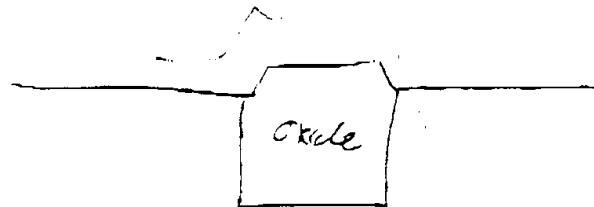
Polish Back to BPSG layer
strip



use act strip BPSG ER is N 50 times
thermal oxide rate so result will be
after strip I



after strip II



BII Polymers 1/26/08

S. Hedges
Dk. 1/26/08

11/15/98
11/16/98

Exhibit B - page 3

STC

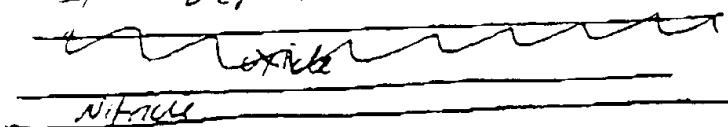
(3)

use thin Nitride for STC

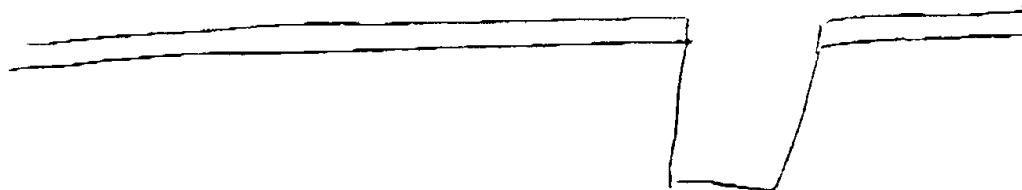
Nitride is used only as a means

to determine oxide height above Si

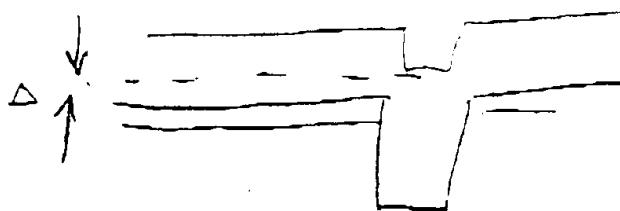
It dep thin Nitrid



II mask and etch



III

dep AlP oxide or PECVD oxide or APCVD
oxide

Thickness is
targeted to
achieve planarity
at ΔA above

Si

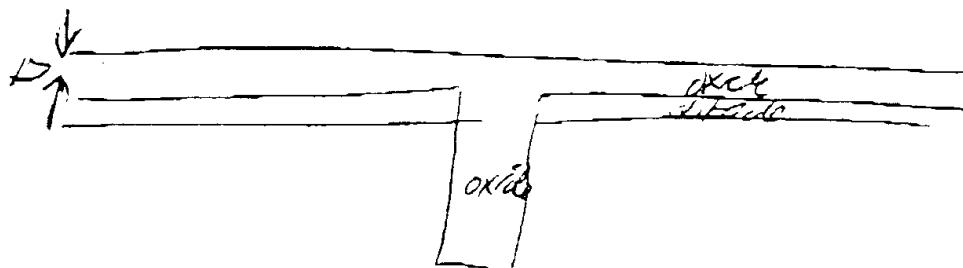
Bill Kauffman - 1/16/99

S. Hedges
Alan Birose11/15/99
11/15/99

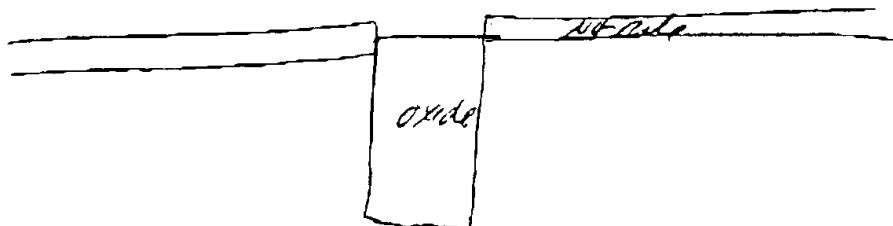
Exhibit B- page 4

~~77~~

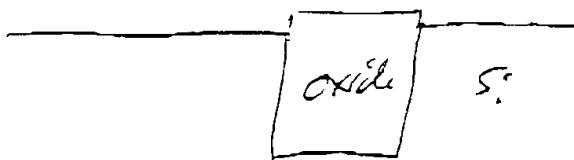
CMB



II wet strip of oxide



III nitrate strip



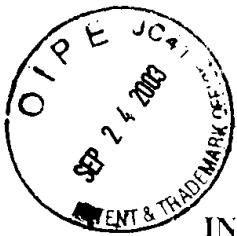
B71 Kowalewski W.L. Miller

S. Hedges
Alvin Stone

10/15/99

10/15/99

Exhibit B - page 5



PATENT
5298-04700/PM00028

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Gilboa et al.

§ Group Art Unit: 1763

§ Examiner: Goudreau, G.

§ Atty. Dkt. No.: 5298-04700

Serial No.: 09/846,119

Filed: April 30, 2001

For: METHOD OF MAKING A
PLANARIZED SEMICONDUCTOR
STRUCTURE

CERTIFICATE OF MAILING
37 C.F.R. § 1.18
I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on the date indicated below.

9-19-03
Date

Kevin L. Daffer

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
Washington, D.C. 20231

I, Yitzhak Gilboa, hereby declare and state that:

1. I am a named inventor in the above-identified patent application, which is U.S. Patent Application No. 09/846,119, filed on April 30, 2001.

2. I have been informed that in the present application, certain claims have been rejected on reference to an article in *Solid State Technology* entitled Improved Planarization for STI with Fixed Abrasive Technology by Vo et al., which was published in June of 2000.

CONCEPTION

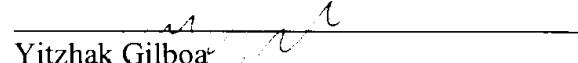
3. As supported below, I, along with Steven Hedayati, William W.C. Koutny, Jr. and Krishnaswamy Ramkumar, conceived of the subject matter claimed in the present application within the United States before June of 2000. The subject matter includes a method for forming a structure within a trench of a semiconductor topography.
4. Exhibit A attached hereto is a true copy of an invention disclosure form and attached pages which bear dates before June of 2000 corresponding to the conception of the invention. The actual dates for the first drawings, the first written description and first oral disclosure to others have been redacted.
5. Page 5 of Exhibit A describes the subject matter of the presently claimed case including the use of fixed abrasive polishing techniques to produce structures with a limited amount of dishing.
6. Exhibit B attached hereto is a true copy of a written description of the conceived subject matter, dated before June of 2000.
7. Page 2 of Exhibit B describes the subject matter of the rejected claims including the use of fixed abrasive polishing techniques to polish a layer deposited within a trench.

REDUCTION TO PRACTICE AND DILIGENCE

8. From at least a time just prior to June of 2000 through the filing of the application on April 30, 2001, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. I did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning just prior to June of 2000 through the filing of the application on April 30, 2001.

9. Upon information and belief, it is my informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as just prior to June of 2000 through the filing of the application on April 30, 2001.

10. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.


Yitzhak Gilboa

Date: 7/14/03

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO PM 00028A. Name ZITZAK, ZBIGNIEW CY Initials ZBZ Empl. No. 22435 Ext. No. 2719Citizenship U.S.A. Dept # 308 Home Phone No. 408-253-2527Home Mailing Address 1761 HERON AVE SCOTTSDALE AZ 85257B. Name William Blawiey CY Initials WKB Empl. No. 135 Ext. No. 2673Citizenship U.S. Dept # Home Phone No. 408-227-0535Home Mailing Address 2555 Homestead #45 Sun. City, AZ 85371
2555 Homestead 45 85371C. Name Steven Healyati CY Initials SH Empl. No. 3534 Ext. No. 4556Citizenship U.S. Dept # 3103 Home Phone No. 408-927-0187Home Mailing Address Syc Valley Quail Circle San Tan CA 951262. TITLE OF INVENTION Method of making Shallow trench isolation Structure

3. CONCEPTION OF INVENTION

- A. Date of first drawing or drawings Redacted
Where can first drawing be found Redacted
- B. Date of first written description Redacted
Where is description found Redacted
- C. Date of first oral disclosure to others Redacted
To whom? Discussed with KTL 5/26/85

4. CONSTRUCTION OF DEVICE

- A. Date Completed _____
 B. Was prototype made? _____
 C. By whom made? _____
 D. Where can the prototype be found? _____

Inventor(s) Z. Zitzak Date 1/24/86Inventor(s) W. Blawiey Date 1/24/86Inventor(s) S. Healyati Date 1/24/86Witnessed, Read, and Understood by: T. L. S. Date 1/24/86Witnessed, Read, and Understood by: L. S. L. Date 1/24/86

Each page upon which information is entered should be signed and witnessed.

Exhibit A - page 1

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

1. INVENTOR(S)

DISCLOSURE NO. _____

A. Name Pankumar CY Initials KTR Empl. No. 3305 Ext. No. 2720
 Citizenship INDIAN Dept # 3108 Home Phone No. (408) 255-1031
 Home Mailing Address 1193 LYNBROOK WAY ; SAN JOSE ; CA 95129

B. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
 Citizenship _____ Dept # _____ Home Phone No. _____
 Home Mailing Address _____

C. Name _____ CY Initials _____ Empl. No. _____ Ext. No. _____
 Citizenship _____ Dept # _____ Home Phone No. _____
 Home Mailing Address _____

2. TITLE OF INVENTION _____

3. CONCEPTION OF INVENTION

- A. Date of first drawing or drawings _____
 Where can first drawing be found _____
- B. Date of first written description _____
 Where is description found _____
- C. Date of first oral disclosure to others _____
 To whom? _____

4. CONSTRUCTION OF DEVICE

- A. Date Completed _____
 B. Was prototype made? _____
 C. By whom made? _____
 D. Where can the prototype be found? _____

Inventor(s): _____ Date: _____

Inventor(s): _____ Date: _____

Inventor(s): _____ Date: _____

Witnessed: Read and Understood by: _____ Date: _____

Witnessed: Read and Understood by: _____ Date: _____
 Each page upon which information is entered should be signed and witnessed

Exhibit A- page 2

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

5. TEST OF DEVICE

- A. Date: Witness(es): _____
B. Results: _____

6. SALE

- A. Was invention sold or offered for sale? Yes No ✓
B. Was invention used to make, assemble or test a commercial product? Yes No ✓
C. Will invention be sold, offered for sale, sampled, or used to make, assemble or test a commercial product? Yes No ✓
D. Actual or estimated date of first sale, offer or commercial use _____
E. Is invention part of a product for which there is a data sheet? Yes No ✓ (If yes, attach a copy)
F. Actual or estimated date of publication, release or availability of data sheet _____

7. USE

- A. Is invention presently being used? Yes No ✓

- B. In what product or process is invention presently being used?

Are there specific plans for its use in near future? In what products or processes?

RAM-D

8. RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS

5,972,792 / 4010573 and 5,782,675 / 5,919,082
4,393,627 / 5,782,675

9. WAS INVENTION Conceived (Yes (No ✓) Constructed (Yes (No ✓) Tested (Yes (No ✓) during performance of Government Contract?

Contract Number _____
(Give Full Contract Number)

=====

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any

Inventor(s): Milton Meltz Date 8/23/00

Inventor(s): J. Hoffman Date 8/23/00

Inventor(s): J. Hoffman Date 8/24/00

Witnessed Read, and Understood by: John J. Hoffman Date 8/24/00

Witnessed Read, and Understood by: US2121 Date 8/24/00

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

FOR ANSWERS TO THE FOLLOWING QUESTIONS, USE THE REMAINDER OF SHEET AND THE ATTACHED SHEET(S).

1. General purpose of invention. State in general terms the objects of the invention.
2. Describe old technology, if any, for performing the function of the invention. Provide references, if available.
3. Indicate the disadvantages of the old technology.
4. Describe your invention and its construction, showing the changes, additions and improvements over the old method.
5. Give details of its operation (i.e., how is your invention used?), if not already described under 4.
6. State the advantages of your invention over what has been done before.
7. Indicate any alternate component(s) and/or method(s) of construction.
8. If a joint invention, indicate what contribution was made by each inventor.
9. Describe the features that are believed to be new.
10. State opinion of relative value of invention.

11. After the disclosure is prepared, it should be signed by the inventor(s) and then read and signed by two witnesses in the space provided at the bottom of each sheet. Forward an electronic copy of this form, as well as a paper copy bearing original signatures, to the Intellectual Property Department.

=====

1. The purpose of the invention is to improve the manufacturability of STI and reduce cost, i.e. via reducing processing steps.
2. Current technology (ST-12 FDS) calls for the following steps:

1. Si → SiO₂ → FDS → ST-12 → ST-5 → Etch → FDS → Conformal
2. SiO₂ → FDS → Etch → SiO₂ → Si → FDS → Conformal

Inventor(s): William Murphy Date: 8/24/02

Inventor(s): J. Daniel Date: 8/24/02

Inventor(s): J. Daniel Date: 8/24/02

Witnessed, Read, and Understood by: John Sadiq Date: 8/24/02

Witnessed, Read, and Understood by: John Sadiq Date: 8/24/02
Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

(3) Disadvantages addressed by invention:

1. Traces width - larger required to overcome resistibility of Poly layer in Poly cap process. This makes low voltage stress difficult.
2. Additional etch required to clean wafer.
3. Extra steps after contact steps which can result in Poly stringing.
4. Another extra film application to overcome steps induced by nitride.

(4) The current invention has three options in using

Fixed, Variable, or 0% as the ~~width~~ method of polish.

The main advantage of fixed polishing is the negligible amount of variation compared to conventional slurry processes. The second advantage is save manufacturing cost due to reduced mask.

Option I - no variable area mask.

In this option the width will be fixed. Film is applied on base and trench. After completion of one stage of this, the trench is opened. After removal of oxide film from the top of the trench and across the center of width of the trench + trench depth variation after each step. Then the base is polished.

Using Fixed Slurry : A standard thickness of 0.500 μ .

The base is polished to a uniformity of 0.0005 μ . The total time required is 0.0005 μ per step.

Inventor(s) Murthy Date 5/26/01

Inventor(s) J. B. Sankar Date 5/26/01

Inventor(s) Praveen Date 5/26/01

Witnessed, Read, and Understood by: John M. H. Sankar Date 5/26/01

Witnessed, Read, and Understood by: L. B. Sankar Date 5/26/01

Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Option II - Deposit Thin Nitride -

Start base oxide growth thin layer of nitride (~500Å)
 Expose TEL oxide mask, Etch back, Deposit 500 Å oxide
 polish down to ~~nitride~~ stop on oxide at a predetermined
 "Residual" oxide where the nitride stops remaining oxide.
 Stop Remaining nitride.

Option II

Start base oxide deposit ~1500 Å, expose ~2000
 Etch back, deposit 500 Å oxide, polish to ~1500 Å layer
 Use wet strip to remove remaining oxide, use of Etch
 with stop to remove oxide, Due to non-TEL Rule
 differences of TEL to oxide etched oxide this is im-
 possible to remove top of nitride, only above 500

- (1) Taking advantage of nitride properties can result in easier
cleaning of the base of voids or in thicker heat sinks.
- (2) Allows for a wider range in design, while keeping around a
thin oxide top subject to polarization problems.

Inventor(s) John Murphy Date 8/24/01Inventor(s) J. Hedges Jr. Date 8/24/01Inventor(s) J. Phillips Date 8/24/01Witnessed, Read, and Understood by: John Murphy Date 8/24/01Witnessed, Read, and Understood by: M. L. Smith Date 8/24/01
Each page upon which information is entered should be signed and witnessed.

CYPRESS SEMICONDUCTOR

CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

- (8) equal contribution
- (9) Fixed abrasive polish, no polish slurry, no separate
polish step
- (10) - Invention will enable reduction of cost of ownership
Compared to Slurry.
- enables STI polish without requirement of large tanks.
- enables STI polish with reduced steps with higher required
for 13 nm lithography.

Inventor(s):	<u>Milton M. Martin</u>	Date:	<u>8-27-02</u>
Inventor(s):	<u>J. Edwards</u>	Date:	<u>8/28/02</u>
Inventor(s):	<u>R. J. Goss</u>	Date:	<u>8/28/02</u>
Witnessed, Read, and Understood by:	<u>John M. Martin</u>	Date:	<u>8/4/02</u>
Witnessed, Read, and Understood by:	<u>RJ Goss</u>	Date:	<u>8/12/02</u>

Each page upon which information is entered should be signed and witnessed.



CYPRESS

Option 1

- No Nitride HM
- Stop after flatness - fixed abrasive
- Wet dip to below Si

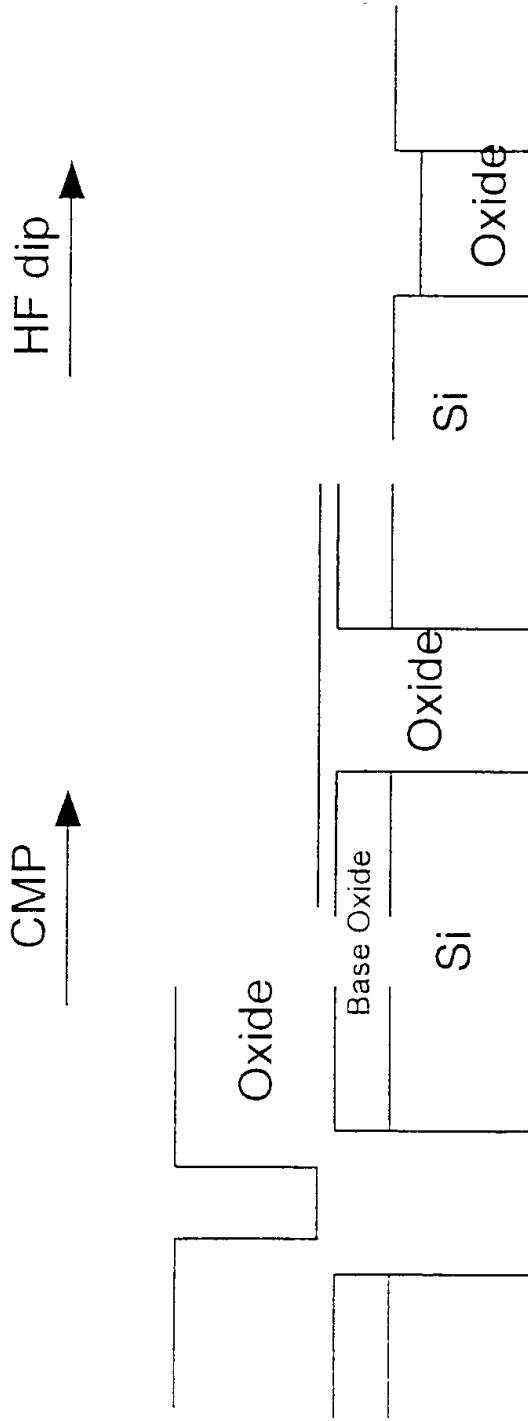


Exhibit A - page 8



STI Invention Disclosure

Method of Making STI

Option 1

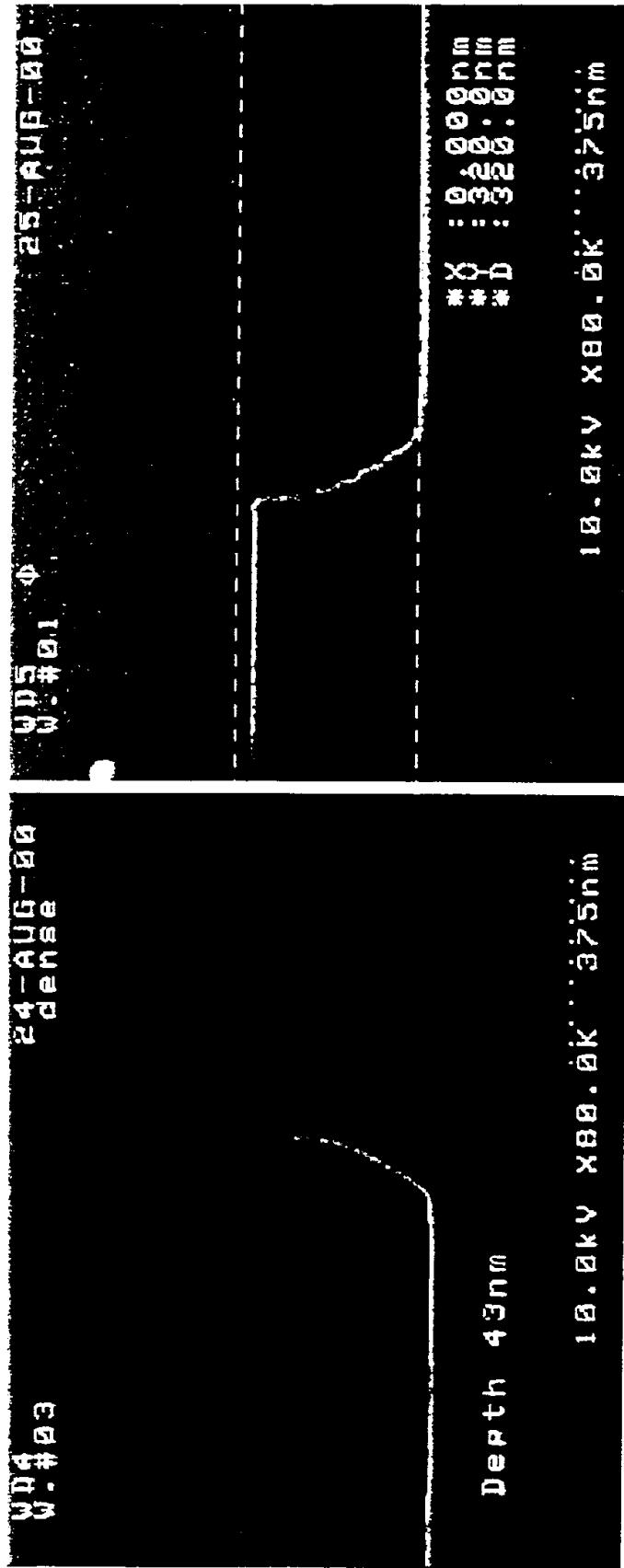


Exhibit A - page 9



CYPRESS

STI Invention Disclosure

Option 2

- Use doped oxide to increase selectivity during wet Dip
- polish to flatness - Fixed Abrasive
- Wet dip - ratio of doped oxide thickness to un-doped thickness controls step height

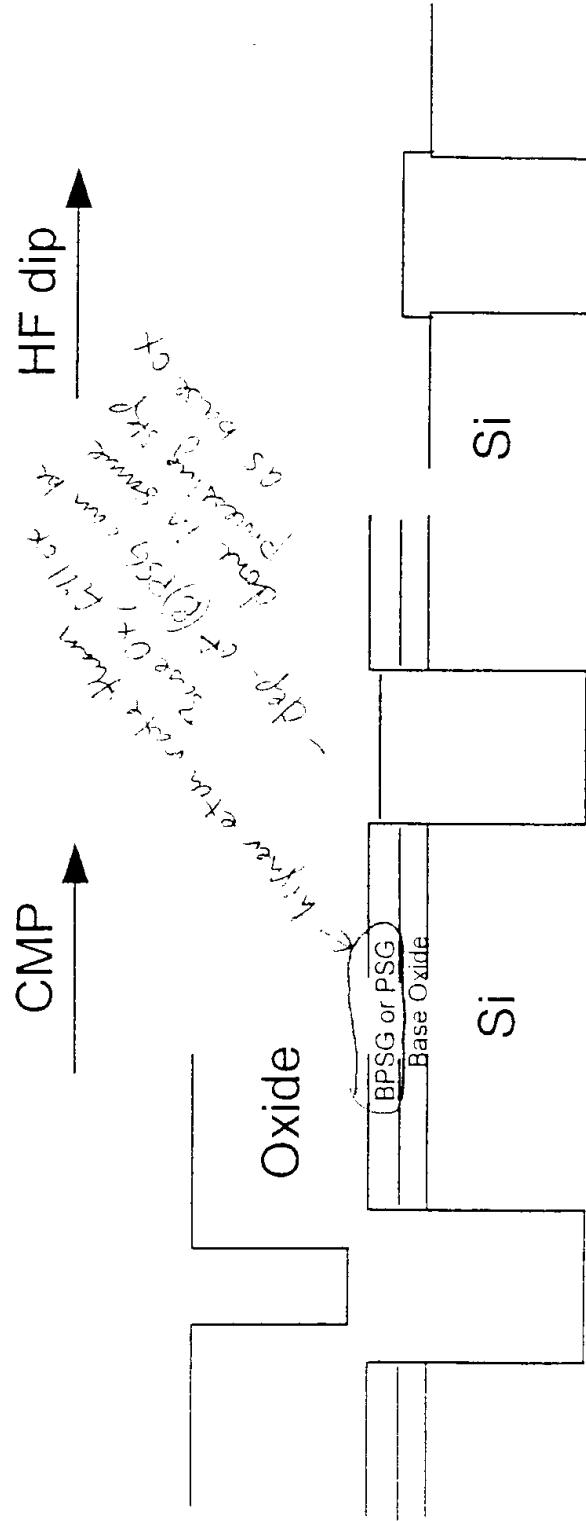


Exhibit A - page 10



CYPRESS

STI Invention Disclosure

Option 3

Low Nitride thickness
with CMP polish stop

- Use thin Nitride
- polish to flatness - Fixed Abrasive ,stop with oxide over Nitride, nitride is used to determine the step height and not as polish stop.
- Wet dip - Nitride thickness controls step height

CMP → HF dip + Nitride Strip →

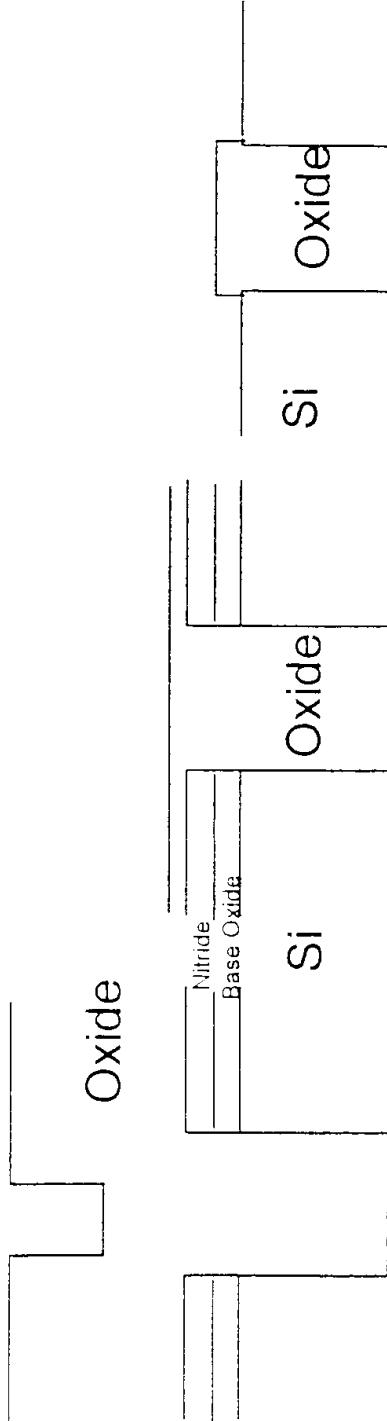
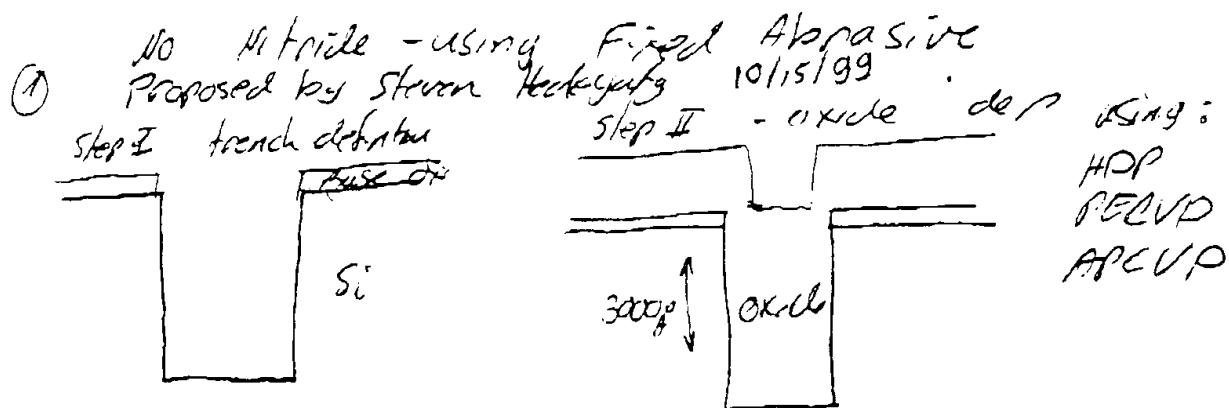


Exhibit A- page 11

STC

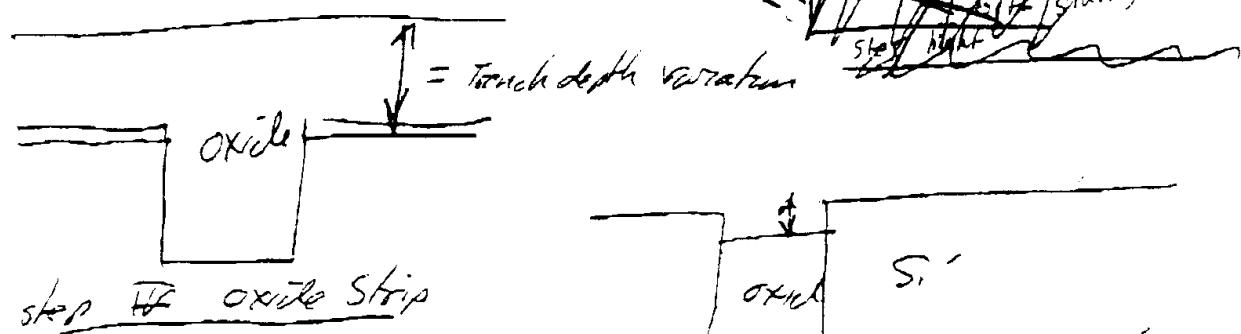
method of making shallow trench isolation
structure with no/or thin nitride CVD stop.



in step II
need to deposit trench depth + trench depth variation

step III Polish

due to Fixed Abrasive properties CVD will self planarize
once flatness is achieved.



Step will result in oxide below Si level

Steven Hedegeorg, Ramkumar, Bill Katney, Mike Albers

S. Hedegeorg
R. Blodorf

11/15/99

11/15/99

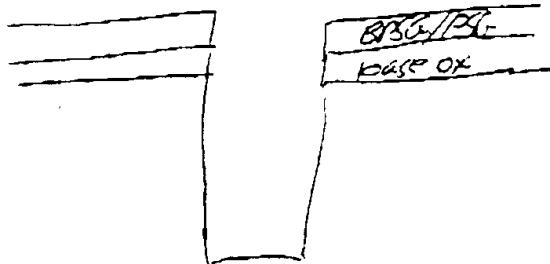
Exhibit B - page 1

500

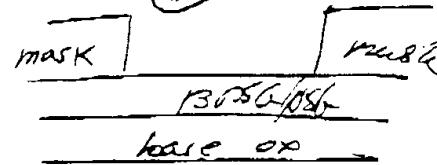
as long as trench depth variations are controlled below a certain number ie $\pm 500 \mu$ then polish can be done without ~~the~~ oxide layer.

(2) ^{2nd} method use of PS/BPSG layer as a base oxide or on top of base oxide

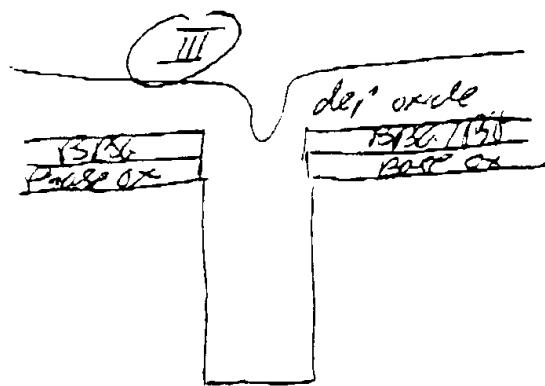
(II)



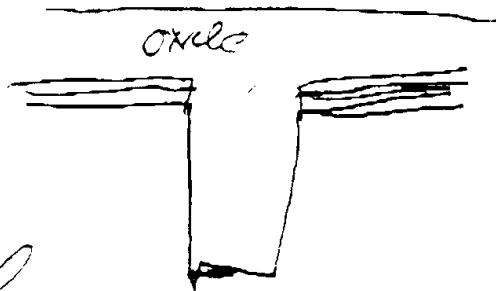
(I)



(III)



Polish using Fixed Abrasive



Bill Kouthey R.K. Jr

S. Hedges
Alan Block

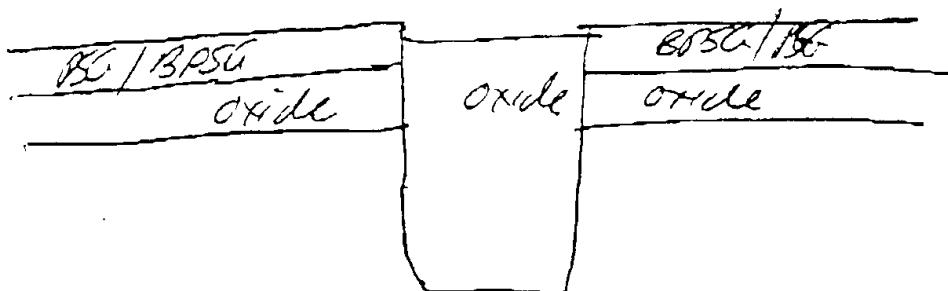
11/15/89
11/15/99

Exhibit B- page 2

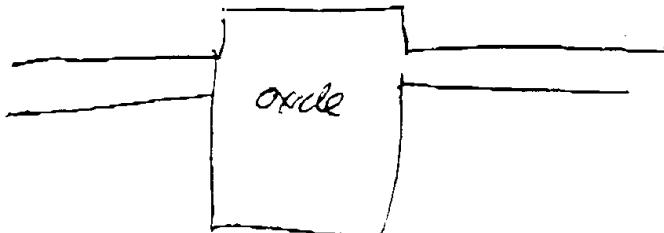
3

~~strip oxide back to BPSG~~

Polish Back to BPSG layer
strip



use act strip BPSG ER is N 50 times
thermal oxide rate so result will be
after strip I



after strip II



BII Courtney 1/2,6 Cello

S. Hedges
Dm. 1/10/00

11/15/98
11/16/98

Exhibit B - page 3

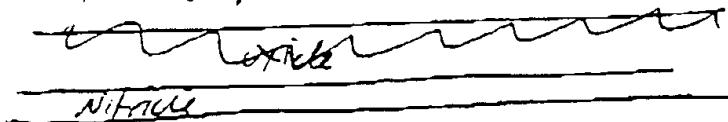
STC

(3)

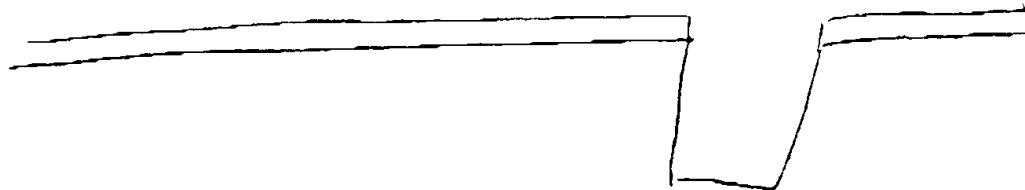
use thin Nitride for STC

Nitride is used only as a means
to determine oxide height above Si

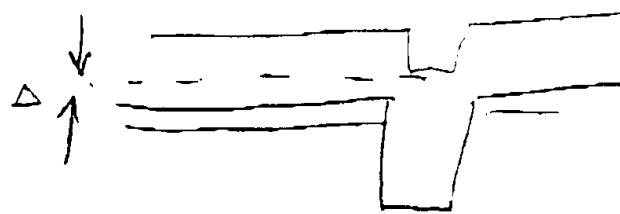
I dep thin Nitride



II mask and etch



III

dep Al₂O₃ oxide or PECVD oxide or APCVD
oxide

Thickness is
targeted to
achieve planarity
at D & above

Si

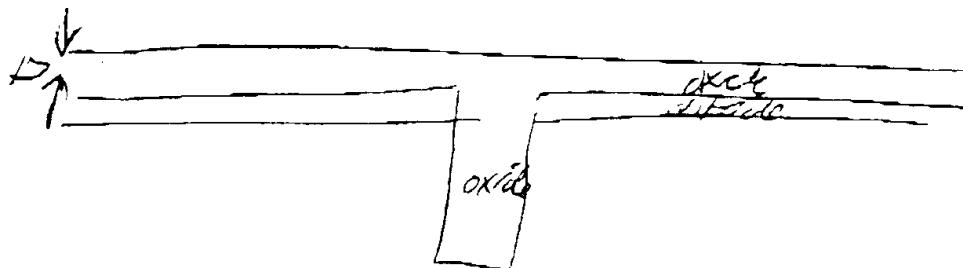
Bill Kauffman - 1/2 hr
of Hedges
Alan Blom

11/15/99 -
11/15/99 -

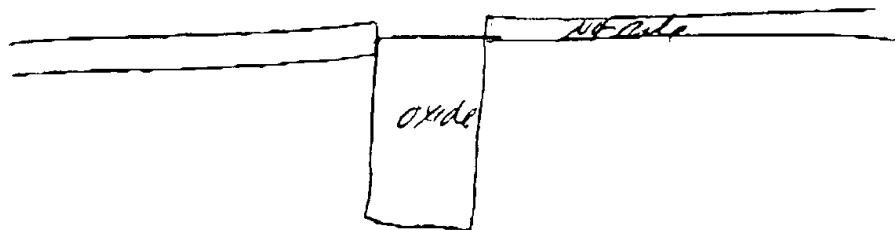
Exhibit B- page 4

~~FF~~

CAB



II wet strip of oxide



III nitrate strip



Bill Kowalsky 1/16/00

S. Hedges
Alvin Stone

10/15/99

10/15/99

Exhibit B - page 5